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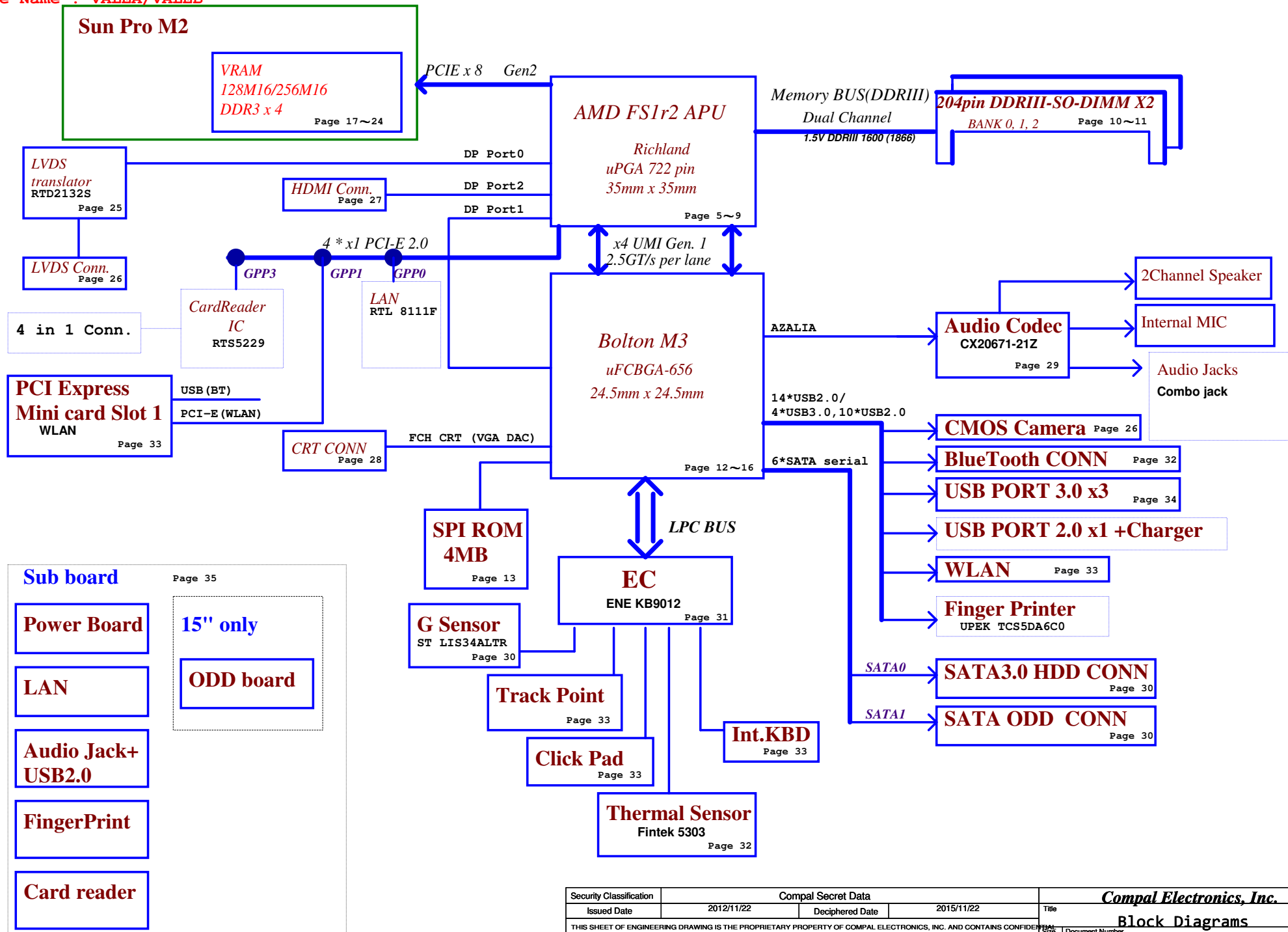
VALEA/VALEB Schematics Document

AMD APU Richland FS1r2 + FCH Bolton-M3 + GPU Sun Pro M2

2012-11-22

REV: 1 . 0

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Issued Date	2012/11/22	Deciphered Date	2015/11/22	Title	Cover Page
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				LA-8126P	1.0
				Date	Sheet
				Tuesday, March 12, 2013	1 of 51



Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+1.5V	1.5V power rail for APU VDDIO and DDR	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.2VS	1.2V (VDDR, VDDP) switched power rail for APU	ON	OFF	OFF
+2.5VS	2.5V for APU VDDA	ON	OFF	OFF
+1.1VALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VGS	1.5V switched power rail	ON	OFF	OFF
+1.8VGS	1.8V switched power rail	ON	OFF	OFF
+0.95VGS	0.95V switched power rail for VGA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS_WLAN	3.3V power rail for WLAN	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001-011xb	15H	F75303 (DDR,VRAM,CPUCORE)	1001-101xb	9AH
			SB-TSI	1001-100xb	98H
			Sun Pro M2	1000-0010b	82H
			LVDS translator		

FCH SMB0

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		
Security ROM		

Stencil Memo

FCH Hudson-M2/3
SATA Port List

SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

Comal
PCIE Port List

APU	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	NC
	PCIE3	Card Reader
FCH	PCIE0	NC
	PCIE1	NC
	PCIE2	NC
	PCIE3	NC

FCH Hudson-M2/3
USB Port List

USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	USB2.0 Port
Port1	NC
Port2	NC
Port3	NC
Port4	NC
Port5	WLAN
Port6	CMOS
Port7	FP
Port8	BT
Port9	NC
Port10	USB 3.0
Port11	USB 3.0
Port12	USB 3.0
Port13	NC

BOM Structure

UMA@ : UMA only
DIS@ : DIS muxless

CMOS@ : USB camera

CONN@ : ME components
X76@, H1G@, S1G@ : VRAM

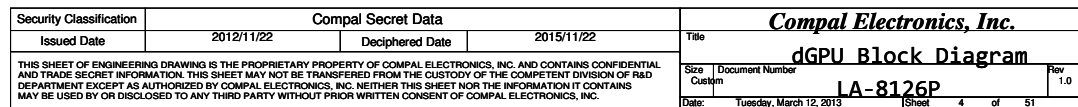
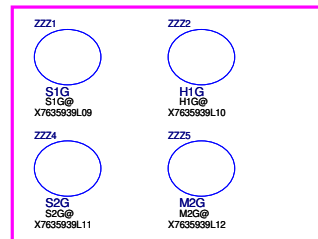
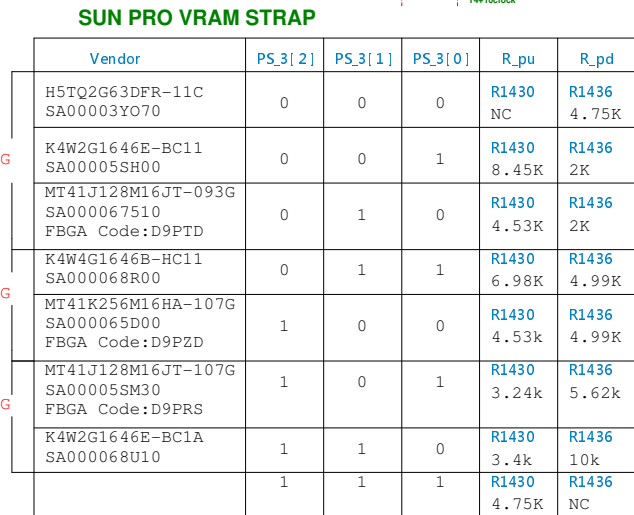
BOM option and stencil

SDV:
CMOS@/DIS@ + X76@

PJ201, PJ401, PJ502, PJ503, PJ504, PJ601, PJ603, PJ604,
PJ701, PJ702, PJ703, PJ704, J1, J2301, J2401, J2402, J2403
PJ402, PJ403, PJ501, PJ602, PJ801, PJ802, PJ803, PJ805

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				Date: Tuesday, March 12, 2013	Sheet 3 of 51	LA-8126P

- All the ASIC supplies, except for VDDR3, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. There is no timing requirement on the ramp up of VDDR3 relative to other power rails.
- The external pull-up resistors on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.



[17] PCIE_CRX_GTX_P[0..7]

[17] PCIE_CRX_GTX_N[0..7]

PCIE_CTX_GRX_P[0..7] [17]

PCIE_CTX_GRX_N[0..7] [17]

JCPU1A

PCI EXPRESS

PCIE_CRX_GTX_P0 AB8
PCIE_CRX_GTX_N0 AB7
PCIE_CRX_GTX_P1 AA9
PCIE_CRX_GTX_N1 AA8
PCIE_CRX_GTX_P2 AA5
PCIE_CRX_GTX_N2 AA6
PCIE_CRX_GTX_P3 Y8
PCIE_CRX_GTX_N3 Y7
PCIE_CRX_GTX_P4 W9
PCIE_CRX_GTX_N4 W8
PCIE_CRX_GTX_P5 W5
PCIE_CRX_GTX_N5 W6
PCIE_CRX_GTX_P6 V8
PCIE_CRX_GTX_N6 V7
PCIE_CRX_GTX_P7 U9
PCIE_CRX_GTX_N7 U8

P_GFX_RXP0
P_GFX_RXN0
P_GFX_TXP1
P_GFX_TXN1
P_GFX_TXP2
P_GFX_TXN2
P_GFX_TXP3
P_GFX_TXN3
P_GFX_TXP4
P_GFX_TXN4
P_GFX_TXP5
P_GFX_TXN5
P_GFX_TXP6
P_GFX_TXN6
P_GFX_TXP7
P_GFX_TXN7
P_GFX_RXP8
P_GFX_RXN8
P_GFX_RXP9
P_GFX_RXN9
P_GFX_RXP10
P_GFX_RXN10
P_GFX_RXP11
P_GFX_RXN11
P_GFX_RXP12
P_GFX_RXN12
P_GFX_RXP13
P_GFX_RXN13
P_GFX_RXP14
P_GFX_RXN14
P_GFX_RXP15
P_GFX_RXN15

GRAPHICS

P_GFX_TXP0
P_GFX_TXN0
P_GFX_TXP1
P_GFX_TXN1
P_GFX_TXP2
P_GFX_TXN2
P_GFX_TXP3
P_GFX_TXN3
P_GFX_TXP4
P_GFX_TXN4
P_GFX_TXP5
P_GFX_TXN5
P_GFX_TXP6
P_GFX_TXN6
P_GFX_TXP7
P_GFX_TXN7
P_GFX_TXP8
P_GFX_TXN8
P_GFX_TXP9
P_GFX_TXN9
P_GFX_TXP10
P_GFX_TXN10
P_GFX_TXP11
P_GFX_TXN11
P_GFX_TXP12
P_GFX_TXN12
P_GFX_TXP13
P_GFX_TXN13
P_GFX_TXP14
P_GFX_TXN14
P_GFX_TXP15
P_GFX_TXN15

AB2 PCIE_CTX_C_GRX_P0 C1 DIS@ 1
AB1 PCIE_CTX_C_GRX_N0 C2 DIS@ 1
AA3 PCIE_CTX_C_GRX_P1 C3 DIS@ 1
AA2 PCIE_CTX_C_GRX_N1 C4 DIS@ 1
Y5 PCIE_CTX_C_GRX_P2 C5 DIS@ 1
Y4 PCIE_CTX_C_GRX_N2 C6 DIS@ 1
Y2 PCIE_CTX_C_GRX_P3 C7 DIS@ 1
Y1 PCIE_CTX_C_GRX_N3 C8 DIS@ 1
W3 PCIE_CTX_C_GRX_P4 C9 DIS@ 1
W2 PCIE_CTX_C_GRX_N4 C10 DIS@ 1
V5 PCIE_CTX_C_GRX_P5 C11 DIS@ 1
V4 PCIE_CTX_C_GRX_N5 C12 DIS@ 1
V2 PCIE_CTX_C_GRX_P6 C13 DIS@ 1
V1 PCIE_CTX_C_GRX_N6 C14 DIS@ 1
U3 PCIE_CTX_C_GRX_P7 C15 DIS@ 1
U2 PCIE_CTX_C_GRX_N7 C16 DIS@ 1

C1 DIS@ 1
C2 DIS@ 1
C3 DIS@ 1
C4 DIS@ 1
C5 DIS@ 1
C6 DIS@ 1
C7 DIS@ 1
C8 DIS@ 1
C9 DIS@ 1
C10 DIS@ 1
C11 DIS@ 1
C12 DIS@ 1
C13 DIS@ 1
C14 DIS@ 1
C15 DIS@ 1
C16 DIS@ 1

2 .1U 0402 16V7K PCIE_CTX_GRX_P0
2 .1U 0402 16V7K PCIE_CTX_GRX_N0
2 .1U 0402 16V7K PCIE_CTX_GRX_P1
2 .1U 0402 16V7K PCIE_CTX_GRX_N1
2 .1U 0402 16V7K PCIE_CTX_GRX_P2
2 .1U 0402 16V7K PCIE_CTX_GRX_N2
2 .1U 0402 16V7K PCIE_CTX_GRX_P3
2 .1U 0402 16V7K PCIE_CTX_GRX_N3
2 .1U 0402 16V7K PCIE_CTX_GRX_P4
2 .1U 0402 16V7K PCIE_CTX_GRX_N4
2 .1U 0402 16V7K PCIE_CTX_GRX_P5
2 .1U 0402 16V7K PCIE_CTX_GRX_N5
2 .1U 0402 16V7K PCIE_CTX_GRX_P6
2 .1U 0402 16V7K PCIE_CTX_GRX_N6
2 .1U 0402 16V7K PCIE_CTX_GRX_P7
2 .1U 0402 16V7K PCIE_CTX_GRX_N7

PCIE_CTX_GRX_P0
PCIE_CTX_GRX_N0
PCIE_CTX_GRX_P1
PCIE_CTX_GRX_N1
PCIE_CTX_GRX_P2
PCIE_CTX_GRX_N2
PCIE_CTX_GRX_P3
PCIE_CTX_GRX_N3
PCIE_CTX_GRX_P4
PCIE_CTX_GRX_N4
PCIE_CTX_GRX_P5
PCIE_CTX_GRX_N5
PCIE_CTX_GRX_P6
PCIE_CTX_GRX_N6
PCIE_CTX_GRX_P7
PCIE_CTX_GRX_N7

SDV/FVT, NO.1

SDV/FVT, NO.1

LAN

WLAN

[35] PCIE_CRX_DTX_P0
[35] PCIE_CRX_DTX_N0
[33] PCIE_CRX_DTX_P1
[33] PCIE_CRX_DTX_N1

Card Reader

[35] PCIE_CRX_DTX_P3
[35] PCIE_CRX_DTX_N3

[12] UMI_RXP0
[12] UMI_RXN0
[12] UMI_RXP1
[12] UMI_RXN1
[12] UMI_RXP2
[12] UMI_RXN2
[12] UMI_RXP3
[12] UMI_RXN3

+1.2VS 1 R1 2 P_ZVDDP 196_0402_1% AG11

AE5 P_GPP_RXP0
AE6 P_GPP_RXN0
AD8 P_GPP_RXP1
AD7 P_GPP_RXN1
AC9 P_GPP_RXP2
AC8 P_GPP_RXN2
AC5 P_GPP_RXP3
AC6 P_GPP_RXN3

GPP

P_GPP_TXP0
P_GPP_TXN0
P_GPP_TXP1
P_GPP_TXN1
P_GPP_TXP2
P_GPP_TXN2
P_GPP_TXP3
P_GPP_TXN3

C33 1
C34 1
C123 1
C124 1
C35 1
C36 1

2 .1U 0402 16V7K PCIE_CTX_DRX_P0
2 .1U 0402 16V7K PCIE_CTX_DRX_N0
2 .1U 0402 16V7K PCIE_CTX_DRX_P1
2 .1U 0402 16V7K PCIE_CTX_DRX_N1
2 .1U 0402 16V7K PCIE_CTX_DRX_P3
2 .1U 0402 16V7K PCIE_CTX_DRX_N3

PCIE_CTX_DRX_P0
PCIE_CTX_DRX_N0
PCIE_CTX_DRX_P1
PCIE_CTX_DRX_N1
PCIE_CTX_DRX_P3
PCIE_CTX_DRX_N3

PCIE_CTX_DRX_P0
PCIE_CTX_DRX_N0
PCIE_CTX_DRX_P1
PCIE_CTX_DRX_N1
PCIE_CTX_DRX_P3
PCIE_CTX_DRX_N3

AG8 P_UMI_RXP0
AG9 P_UMI_RXN0
AG6 P_UMI_RXP1
AG5 P_UMI_RXN1
AF7 P_UMI_RXP2
AF6 P_UMI_RXN2
AE8 P_UMI_RXP3
AE9 P_UMI_RXN3

UMI

P_UMI_TXP0
P_UMI_TXN0
P_UMI_TXP1
P_UMI_TXN1
P_UMI_TXP2
P_UMI_TXN2
P_UMI_TXP3
P_UMI_TXN3

C37 1
C38 1
C39 1
C40 1
C41 1
C42 1
C43 1
C44 1

2 .1U 0402 16V7K UMI_TXP0_C
2 .1U 0402 16V7K UMI_TXN0_C
2 .1U 0402 16V7K UMI_TXP1_C
2 .1U 0402 16V7K UMI_TXN1_C
2 .1U 0402 16V7K UMI_TXP2_C
2 .1U 0402 16V7K UMI_TXN2_C
2 .1U 0402 16V7K UMI_TXP3_C
2 .1U 0402 16V7K UMI_TXN3_C

UMI_TXP0 [12]
UMI_TXN0 [12]
UMI_TXP1 [12]
UMI_TXN1 [12]
UMI_TXP2 [12]
UMI_TXN2 [12]
UMI_TXP3 [12]
UMI_TXN3 [12]

Power Sequence of APU

+1.5V

+2.5VS

+1.5VS

+APU_CORE

+APU_CORE_NB

+1.2VS

Group A

Group B

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				LA-8126P	1.0
Date: Tuesday, March 12, 2013				Sheet	5 of 51

Place near APU

[25] DP0_TXP0_C
[25] DP0_TXN0_C

C52 1 2 .1U 0402 16V7K DP0_TXP0 L3
C47 1 2 .1U 0402 16V7K DP0_TXN0 L2

[13] ML_VGA_TXP0
[13] ML_VGA_TXN0

C61 1 2 .1U 0402 16V7K DP1_TXP0 H5
C62 1 2 .1U 0402 16V7K DP1_TXN0 H4

[13] ML_VGA_TXP1
[13] ML_VGA_TXN1

C63 1 2 .1U 0402 16V7K DP1_TXP1 H2
C64 1 2 .1U 0402 16V7K DP1_TXN1 H1

[13] ML_VGA_TXP2
[13] ML_VGA_TXN2

C65 1 2 .1U 0402 16V7K DP1_TXP2 G3
C66 1 2 .1U 0402 16V7K DP1_TXN2 G2

[13] ML_VGA_TXP3
[13] ML_VGA_TXN3

C67 1 2 .1U 0402 16V7K DP1_TXP3 F2
C68 1 2 .1U 0402 16V7K DP1_TXN3 F1

[27] HDMI_TX2P
[27] HDMI_TX2N

C50 1 2 .1U 0402 16V7K DP2_TXP0 L9
C51 1 2 .1U 0402 16V7K DP2_TXN0 L8

[27] HDMI_TX1P
[27] HDMI_TX1N

C55 1 2 .1U 0402 16V7K DP2_TXP1 L5
C56 1 2 .1U 0402 16V7K DP2_TXN1 L6

[27] HDMI_TX0P
[27] HDMI_TX0N

C57 1 2 .1U 0402 16V7K DP2_TXP2 K8
C58 1 2 .1U 0402 16V7K DP2_TXN2 K7

[27] HDMI_CLKP
[27] HDMI_CLKN

C59 1 2 .1U 0402 16V7K DP2_TXP3 J6
C60 1 2 .1U 0402 16V7K DP2_TXN3 J5

[12] APU_CLK
[12] APU_CLK#

AE11
AD11

[12] APU_DISP_CLK
[12] APU_DISP_CLK#

AB11
AA11

[45] APU_SVC
[45] APU_SVD

B3
A3

[45] APU_SVT

C3

[12] APU_RST#
[12,45] APU_PWRGD

AF10
AB12

[12] APU_PROCHOT#
[12] APU_THERMTRIP#

AE12
AF12

[45] APU_VDD_SEN_L
[45] APU_VDDNB_SEN

B4
A4

[45] APU_VDD_SEN_H

B5
A5

Route as differential
with VSS_SENSE

T20
T21

[45] APU_VDD_SEN_L
[45] APU_VDDNB_SEN

B4
A4

[45] APU_VDD_SEN_H

B5
A5

[45] APU_VDD_SEN_L
[45] APU_VDDNB_SEN

B4
A4

[45] APU_VDD_SEN_H

B5
A5

[45] APU_VDD_SEN_L
[45] APU_VDDNB_SEN

B4
A4

[45] APU_VDD_SEN_H

B5
A5

[45] APU_VDD_SEN_L
[45] APU_VDDNB_SEN

B4
A4

[45] APU_VDD_SEN_H

B5
A5

[45] APU_VDD_SEN_L
[45] APU_VDDNB_SEN

B4
A4

[45] APU_VDD_SEN_H

B5
A5

[45] APU_VDD_SEN_L
[45] APU_VDDNB_SEN

B4
A4

[45] APU_VDD_SEN_H

B5
A5

[45] APU_VDD_SEN_L
[45] APU_VDDNB_SEN

B4
A4

[45] APU_VDD_SEN_H

B5
A5

[45] APU_VDD_SEN_L
[45] APU_VDDNB_SEN

B4
A4

[45] APU_VDD_SEN_H

B5
A5

[45] APU_VDD_SEN_L
[45] APU_VDDNB_SEN

B4
A4

[45] APU_VDD_SEN_H

B5
A5

[45] APU_VDD_SEN_L
[45] APU_VDDNB_SEN

B4
A4

[45] APU_VDD_SEN_H

B5
A5

JCPU1D

ANALOG/DISPLAY/MISC

LVDS

DISPLAY PORT 0

DISPLAY PORT 1

DISPLAY PORT 2

TEST

SERIAL

CTRL

JTAG

SENSE

JCPU1D

ANALOG/DISPLAY/MISC

LVDS

DISPLAY PORT 0

DISPLAY PORT 1

DISPLAY PORT 2

TEST

SERIAL

CTRL

JTAG

SENSE

JCPU1D

ANALOG/DISPLAY/MISC

LVDS

DISPLAY PORT 0

DISPLAY PORT 1

DISPLAY PORT 2

TEST

SERIAL

CTRL

JTAG

SENSE

JCPU1D

ANALOG/DISPLAY/MISC

LVDS

DISPLAY PORT 0

DISPLAY PORT 1

DISPLAY PORT 2

TEST

SERIAL

CTRL

JTAG

SENSE

JCPU1D

ANALOG/DISPLAY/MISC

LVDS

DISPLAY PORT 0

DISPLAY PORT 1

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ANALOG/DISPLAY/MISC

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JCPU1D

ANALOG/DISPLAY/MISC

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ANALOG/DISPLAY/MISC

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DISPLAY PORT 0

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ANALOG/DISPLAY/MISC

LVDS

DISPLAY PORT 0

DISPLAY PORT 1

DISPLAY PORT 2

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SERIAL

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JTAG

SENSE

JCPU1D

ANALOG/DISPLAY/MISC

LVDS

DISPLAY PORT 0

DISPLAY PORT 1

DISPLAY PORT 2

TEST

SERIAL

CTRL

JTAG

SENSE

JCPU1D

ANALOG/DISPLAY/MISC

LVDS

DISPLAY PORT 0

DISPLAY PORT 1

DISPLAY PORT 2

TEST

SERIAL

CTRL

JTAG

SENSE

JCPU1D

ANALOG/DISPLAY/MISC

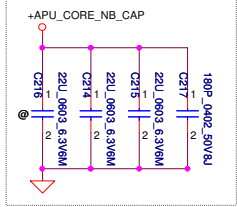
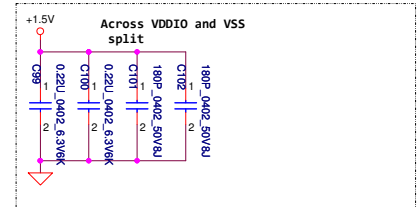
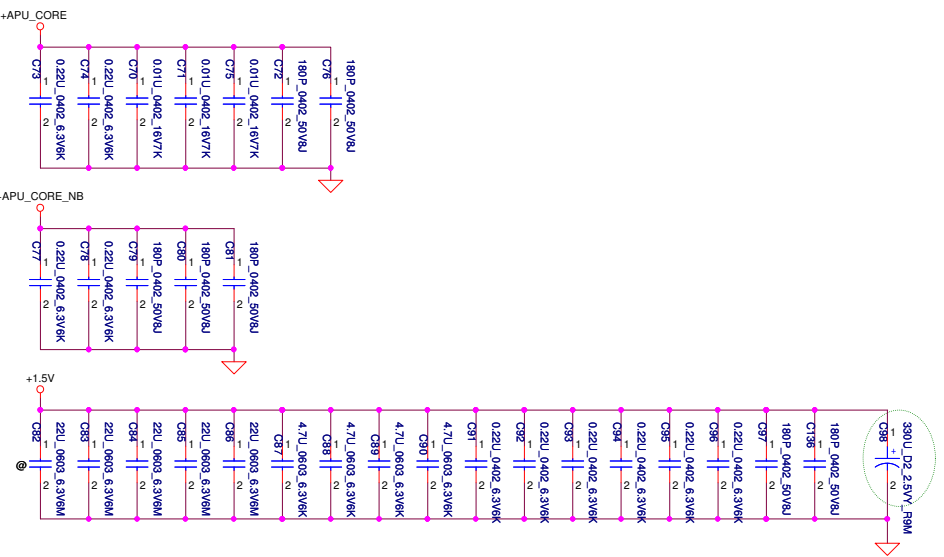
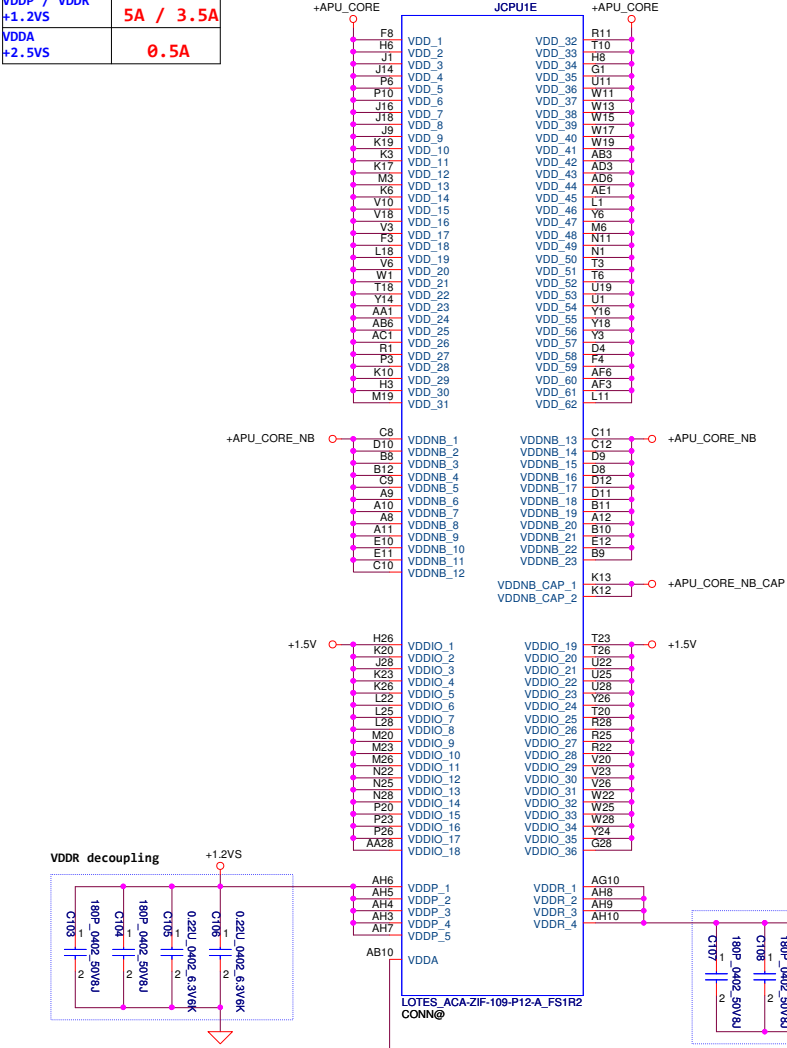
LVDS

DISPLAY PORT 0

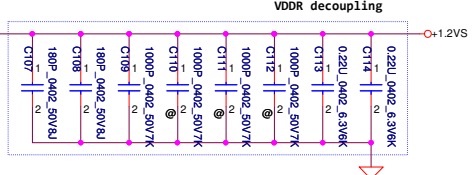
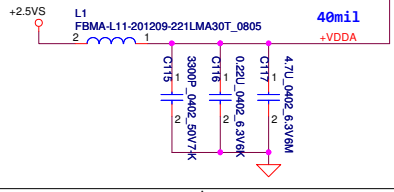
DISPLAY PORT 1

DISPLAY PORT 2

Power Name	Consumption
VDD	
+APU_CORE	60A
VDDNB	
+APU_CORE_NB	44A
VDDIO	
+1.5V	3.2A
VDDP / VDDR	
+1.2VS	5A / 3.5A
VDDA	
+2.5VS	0.5A



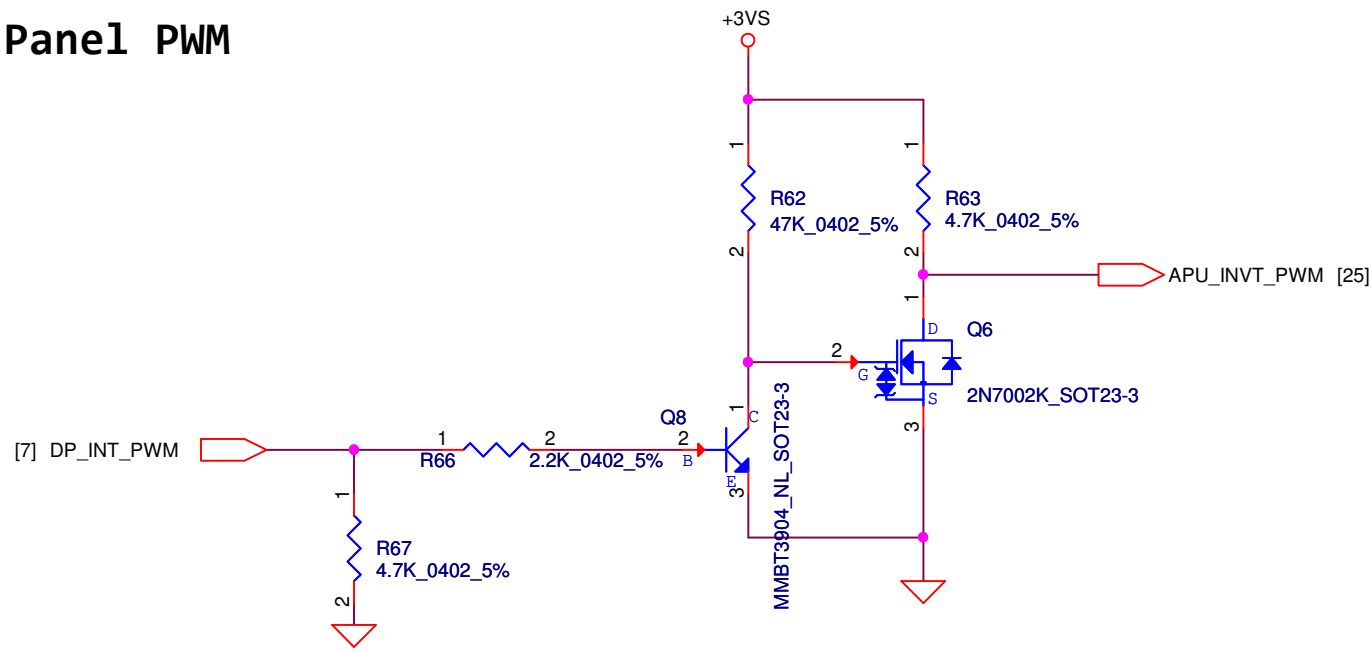
JCPU1F			
J20	VSS_1	VSS_73	A19
L4	VSS_2	VSS_74	A21
R7	VSS_3	VSS_75	A23
W18	VSS_4	VSS_76	A25
A15	VSS_5	VSS_77	A7
AB17	VSS_6	VSS_78	AA4
AC22	VSS_7	VSS_79	AB13
AF24	VSS_8	VSS_80	AB15
AH23	VSS_9	VSS_81	AB19
AH25	VSS_10	VSS_82	AB21
B7	VSS_11	VSS_83	AB23
C14	VSS_12	VSS_84	AB25
C16	VSS_13	VSS_85	AB27
C20	VSS_14	VSS_86	AB9
C22	VSS_15	VSS_87	AC14
C24	VSS_16	VSS_88	AC15
C26	VSS_17	VSS_89	AC18
C28	VSS_18	VSS_90	AC20
D13	VSS_19	VSS_91	AC24
D15	VSS_20	VSS_92	AC28
D17	VSS_21	VSS_93	AC28
D19	VSS_22	VSS_94	AC4
D23	VSS_23	VSS_95	AC7
D25	VSS_24	VSS_96	AD9
D27	VSS_25	VSS_97	AE13
E4	VSS_26	VSS_98	AE15
E9	VSS_27	VSS_99	AE17
F14	VSS_28	VSS_100	AE7
F16	VSS_29	VSS_101	N10
F18	VSS_30	VSS_102	N4
F20	VSS_31	VSS_103	N7
F22	VSS_32	VSS_104	N10
F24	VSS_33	VSS_105	R4
F26	VSS_34	VSS_106	T11
F28	VSS_35	VSS_107	T9
G13	VSS_36	VSS_108	U10
G15	VSS_37	VSS_109	U18
G17	VSS_38	VSS_110	U4
G19	VSS_39	VSS_111	U7
G21	VSS_40	VSS_112	V11
G23	VSS_41	VSS_113	AE19
G25	VSS_42	VSS_114	AE23
G4	VSS_43	VSS_115	AE25
J22	VSS_44	VSS_116	AE27
J24	VSS_45	VSS_117	AE4
J4	VSS_46	VSS_118	AE7
J7	VSS_47	VSS_119	AF14
K11	VSS_48	VSS_120	AF16
K14	VSS_49	VSS_121	AF18
K9	VSS_50	VSS_122	AF20
AC11	VSS_51	VSS_123	AF22
L19	VSS_52	VSS_124	AF26
L7	VSS_53	VSS_125	AF28
MT1	VSS_54	VSS_126	AF9
AF11	VSS_55	VSS_127	AG4
V19	VSS_56	VSS_128	AG7
V9	VSS_57	VSS_129	AH13
W16	VSS_58	VSS_130	AH15
W4	VSS_59	VSS_131	AH17
W7	VSS_60	VSS_132	AH19
Y11	VSS_61	VSS_133	AH21
Y20	VSS_62	VSS_134	P9
Y22	VSS_63	VSS_135	C18
Y9	VSS_64	VSS_136	D21
A17	VSS_65	VSS_137	W14
A13	VSS_66	VSS_138	P11
K16	VSS_67	VSS_139	C7
F24	VSS_68	VSS_140	E8
G8	VSS_69	VSS_141	K18
H7	VSS_70	VSS_142	W12
J8	VSS_71	VSS_143	
	VSS_72	VSS_144	



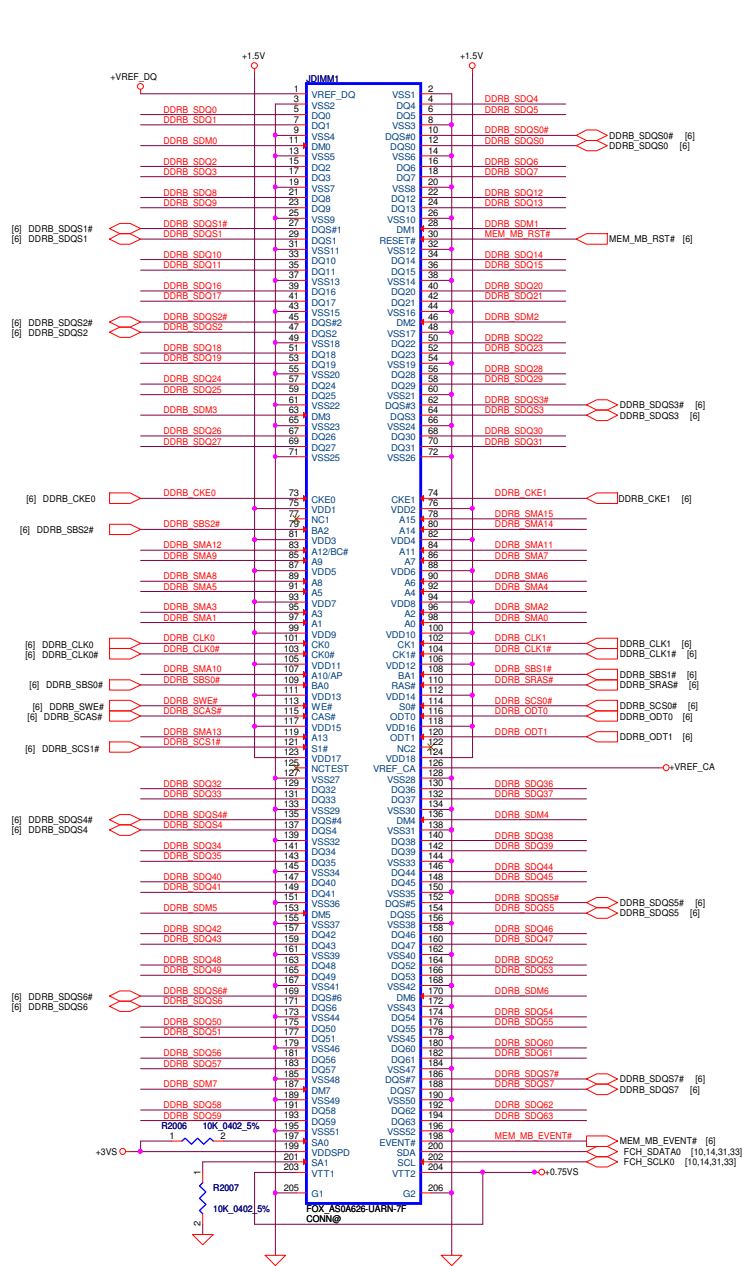
Demo Board Capacitor			
APU_CORE	CORE_NB	CORE_NB_CAP	VDDIO_SUS
22uF x 10	22uF x 2	22uF x 2	(CPU side)
0.22uF x 2	10uF x 1	180pF x 1	22uF x 4
0.01uF x 3	0.22uF x 2		4.7uF x 4
180pF x 2	180pF x 3		0.22uF x 6 +2(split)
			180pF x 1 + 2(split)
VDDP	VDDR	VDDA	VDDIO_SUS
0.22uF x 2	0.22uF x 2	4.7uF x 1	(DIMM x2)
180pF x 2	1nF x 4	0.22uF x 1	100uF x 2
	180pF x 2	3.3nF x 1	0.1uF x 12

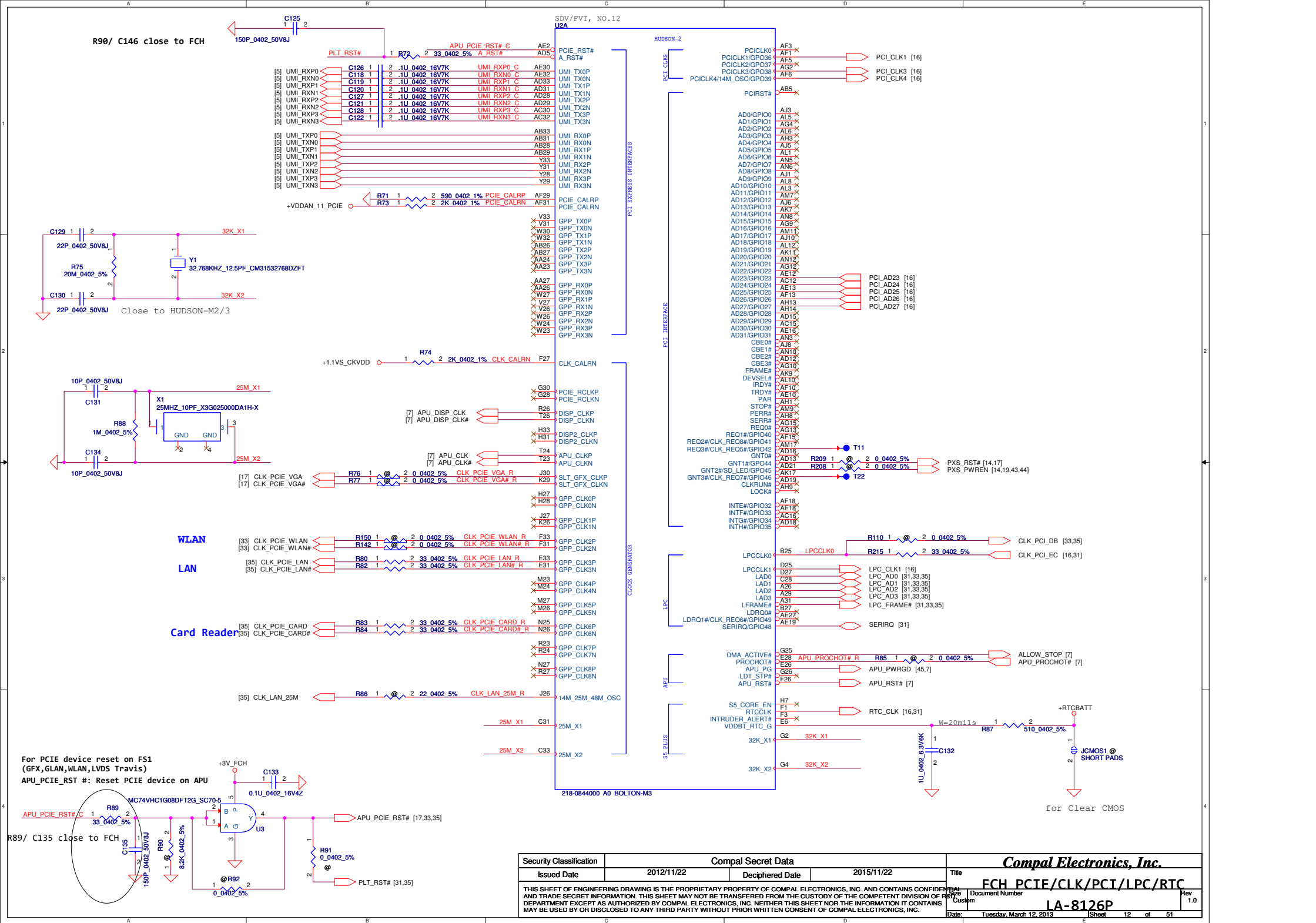
Security Classification		Compal Secret Data		Title	
Issued Date	2012/11/22	Deciphered Date	2015/11/22	FS1r2 PWR/GND	
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Date: Tuesday, March 12, 2013				Sheet	8 of 51

Panel PWM



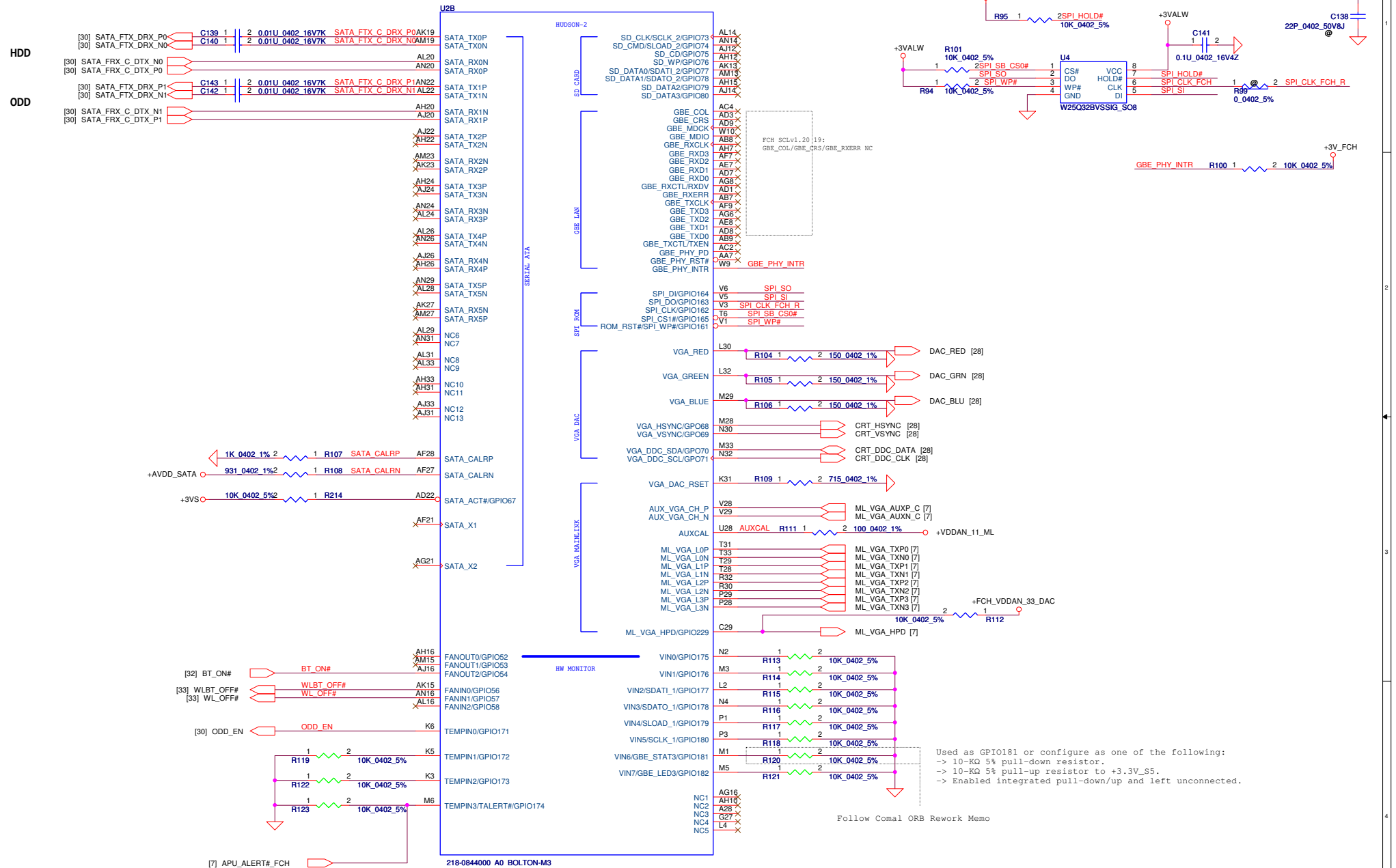
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/11/22	Deciphered Date	2015/11/22	Title	FS1r2 Signal Level Shifter
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				Rev	1.0
Date:		Tuesday, March 12, 2013		Sheet	9 of 51



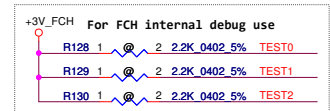
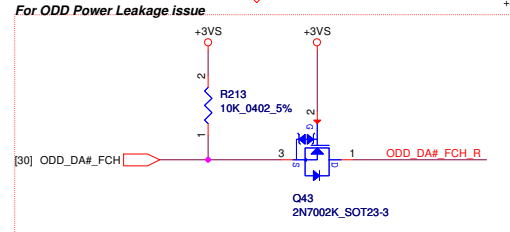
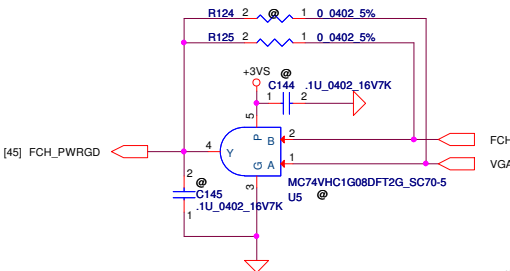


Security Classification		Compal Secret Data		Compal Electronics, Inc. FCH PCIE/CLK/PCI/LPC/RTC	
Issued Date	2012/11/22	Deciphered Date	2015/11/22	Title	
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Date: Tuesday, March 12, 2013				Sheet	12 of 51

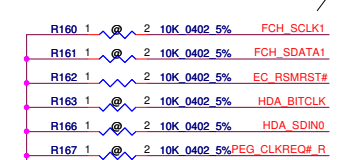
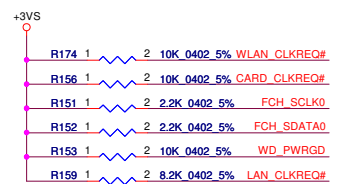
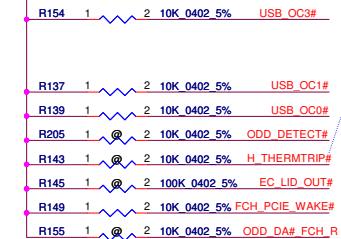
**4MB SPI ROM
& Non-share ROM.**



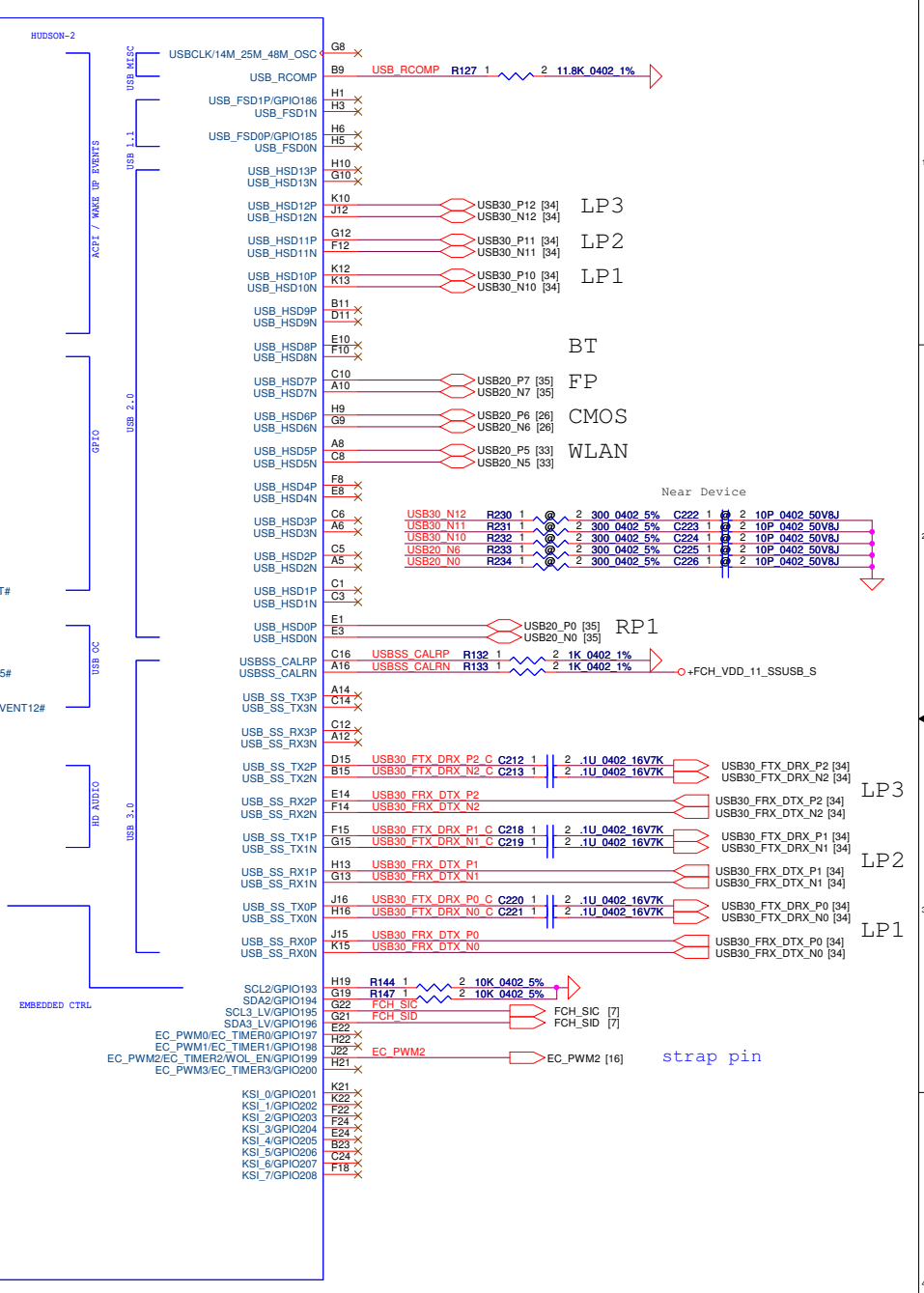
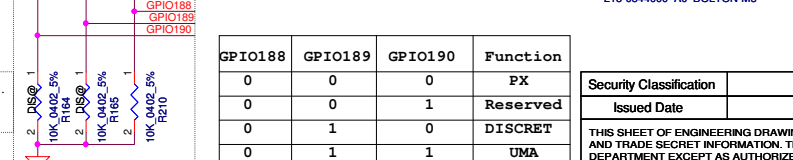
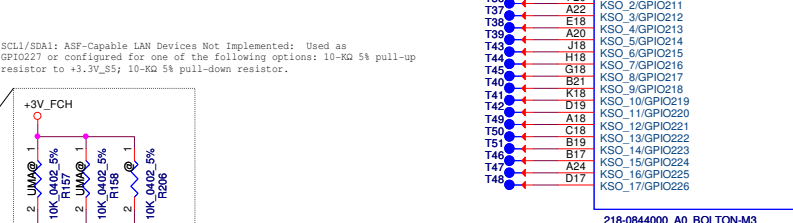
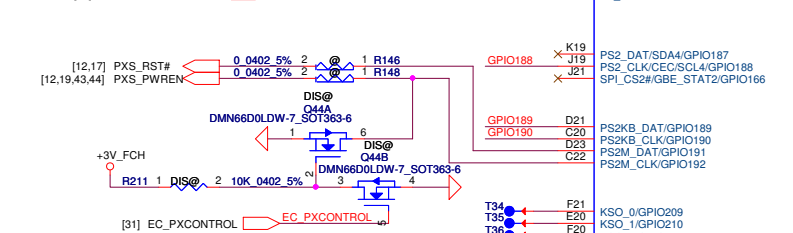
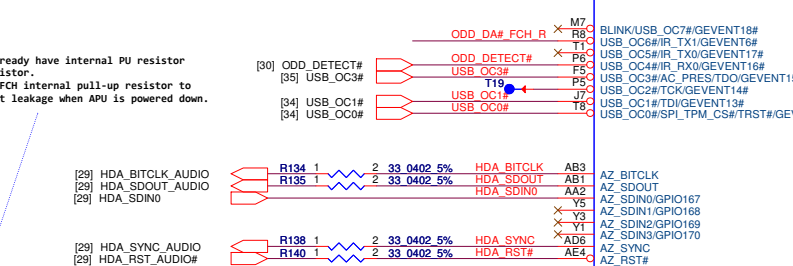
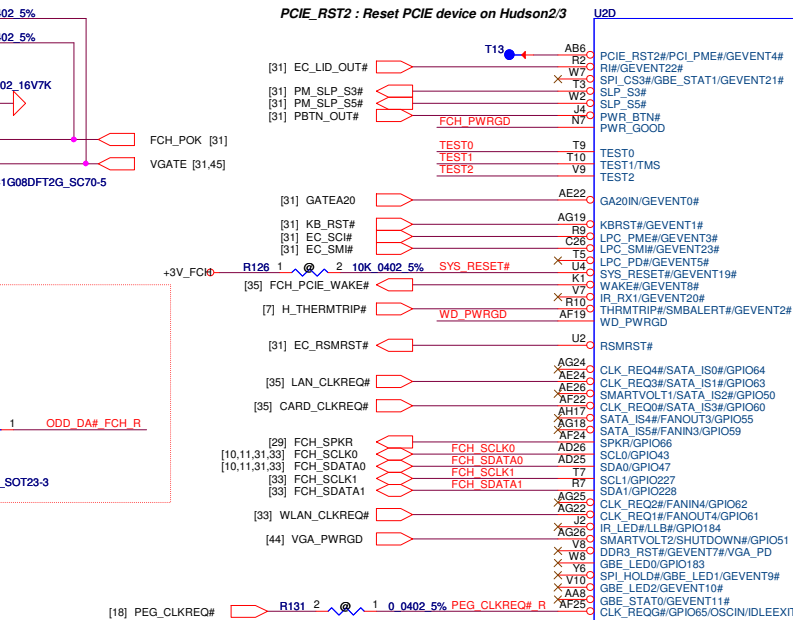
Security Classification		Compal Secret Data		Compal Electronics, Inc. FCH SATA/SPT/VGA/HWM/SD	
Issued Date	2012/11/22	Deciphered Date	2015/11/22	Title	
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Date: Tuesday, March 12, 2013				Sheet	13 of 51



THERRMTRIP
8/16 AMD confirmed: The FCH already have internal PU resistor and don't need external PU resistor.
Note: need BIOS check: Ensure FCH internal pull-up resistor to +3.3V S5 is disabled to prevent leakage when APU is powered down.

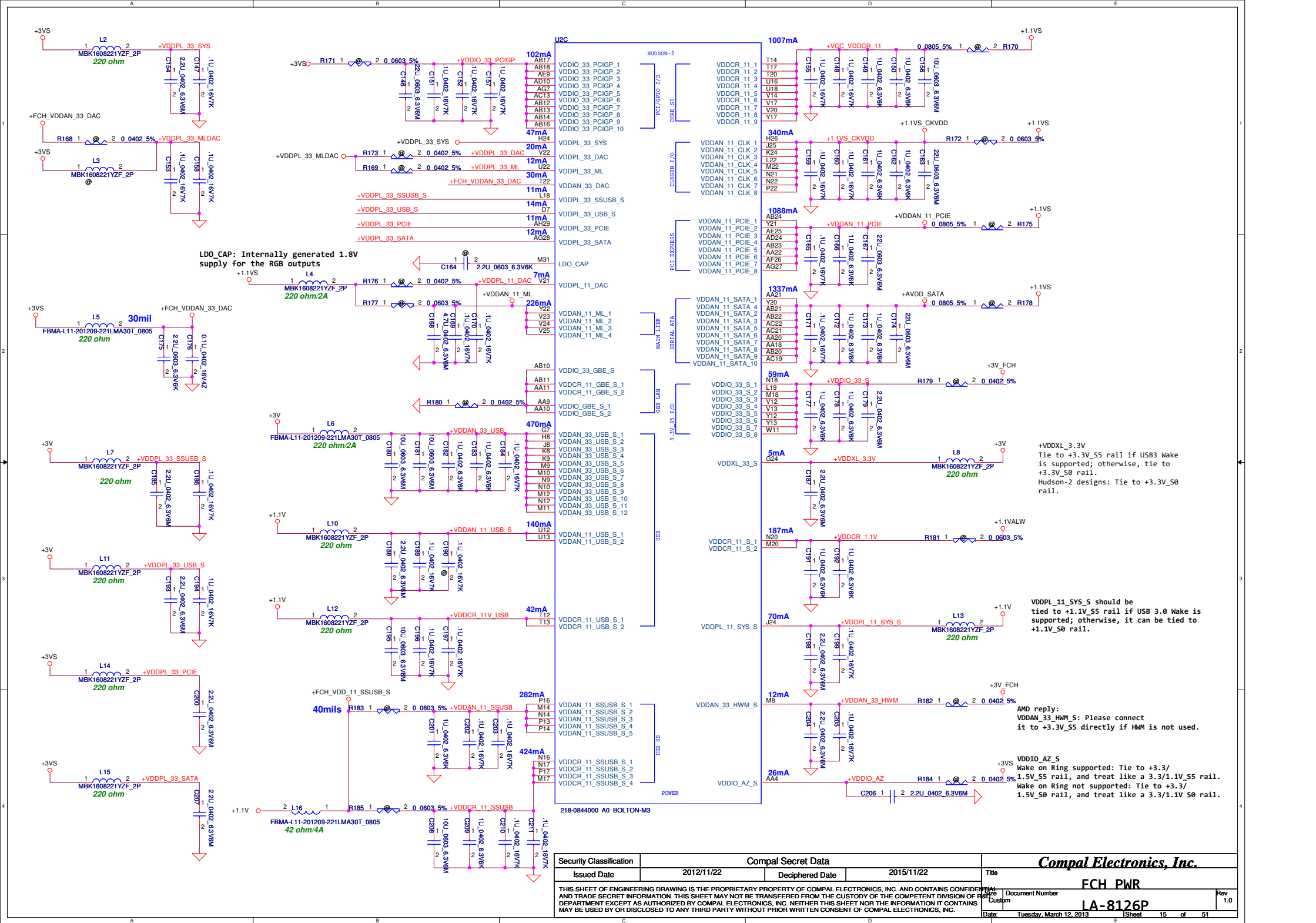


CLKREQ# Not Implemented:
Used as GPIO65, IDLEEXIT#, or left unconnected.



GPIO188	GPIO189	GPIO190	Function
0	0	0	PX
0	0	1	Reserved
0	1	0	DISCRET
0	1	1	UMA

Security Classification	Compal Secret Data			Date		Page	
Issued Date	2012/11/22	Deciphered Date	2015/11/22	Title	Document Number	Rev	1.0
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				Compal Electronics, Inc.			
				FCH_SATA/SPI/VGA/HWM/SD			
				LA-8126P			
				Date: Tuesday, March 12, 2013			

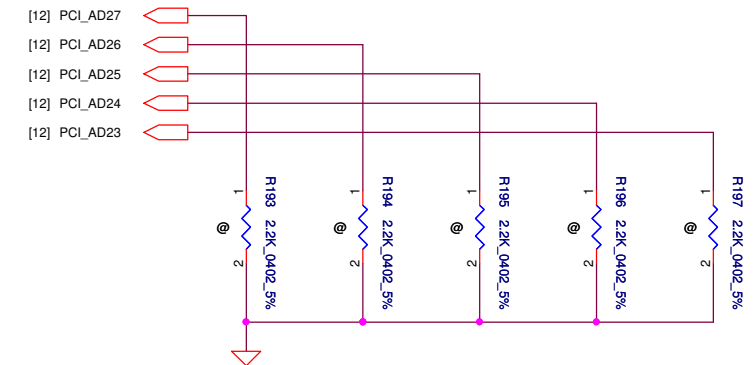
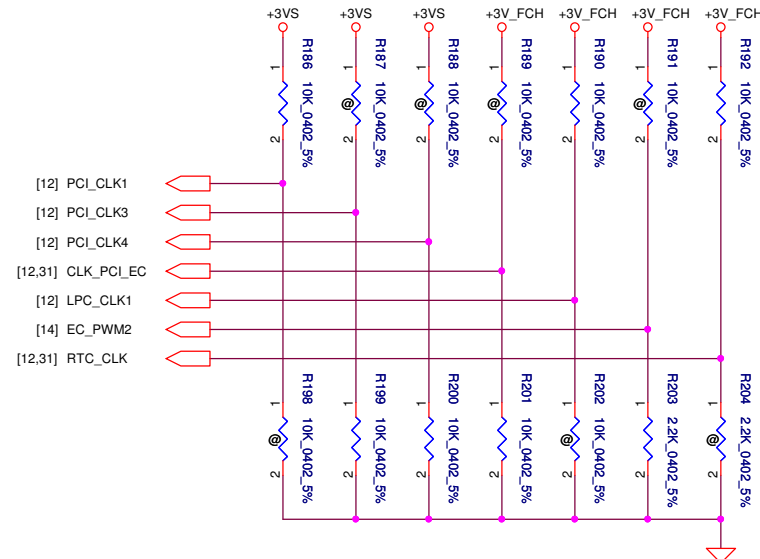
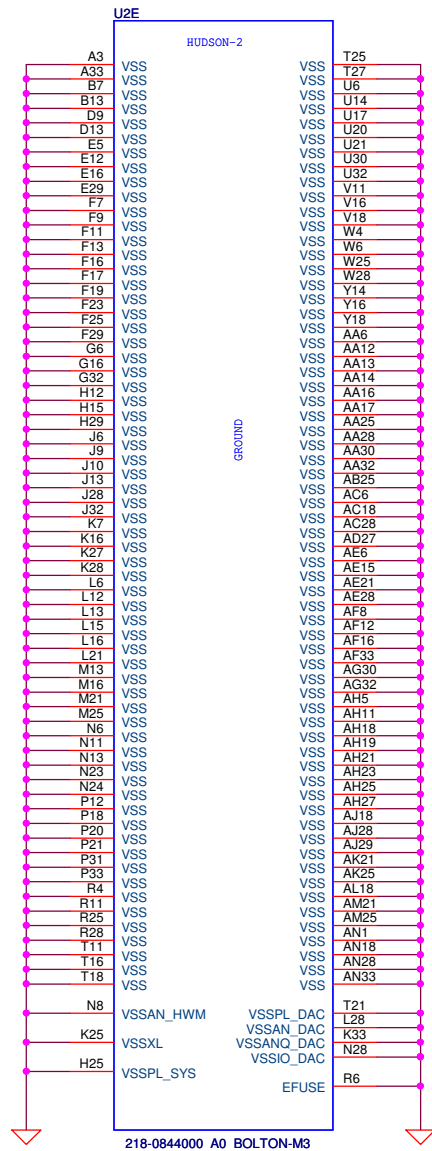


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Issued Date	2012/11/22	Deciphered Date	2015/11/22	Title	FCH PWR				
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				Custom	LA-8126P				1.0
Date:	Tuesday, March 12, 2013	Sheet	15	of	51				

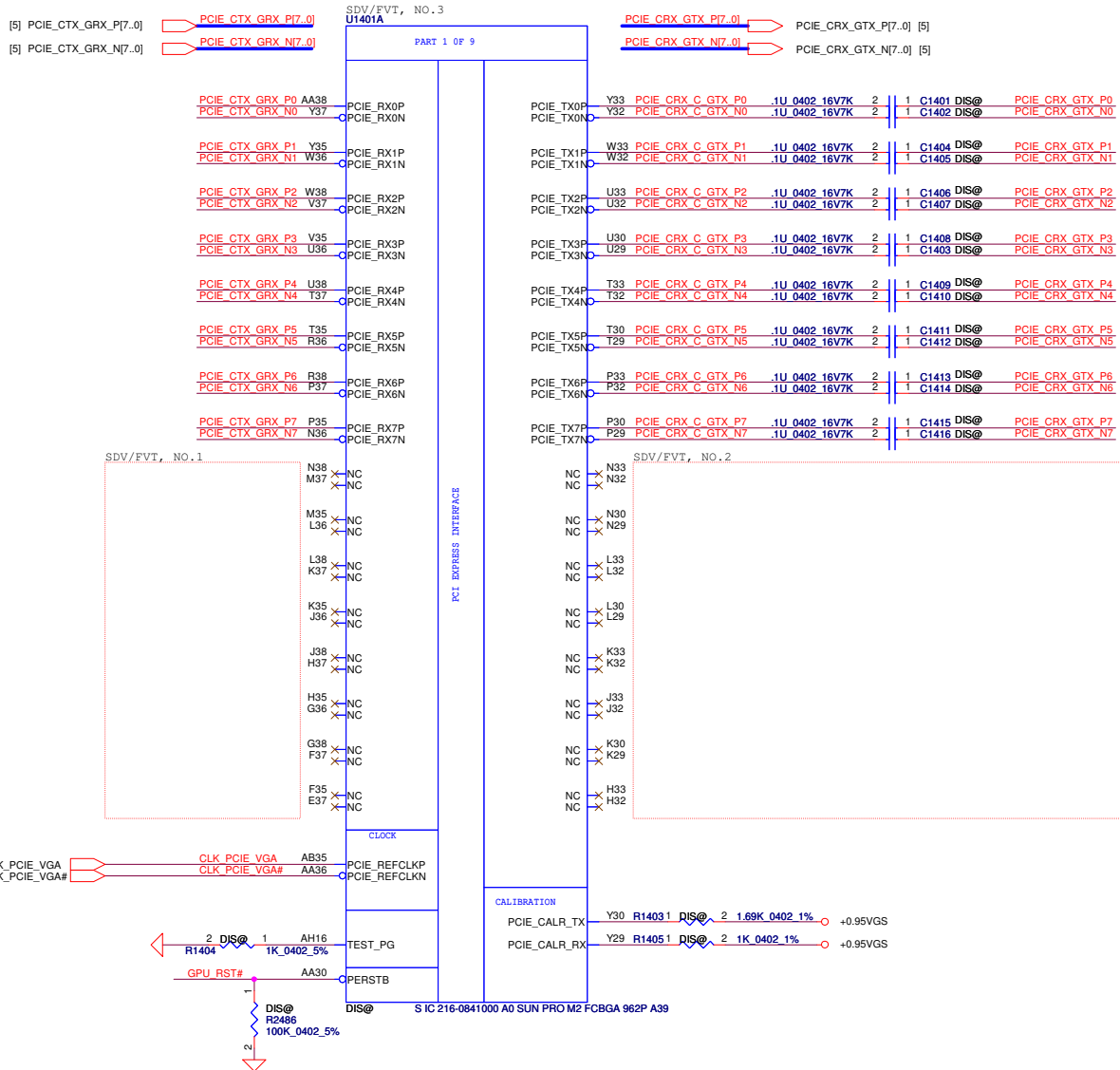
FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

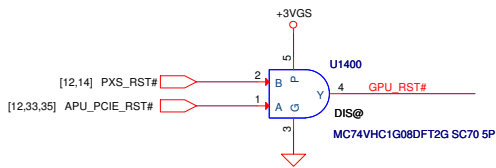
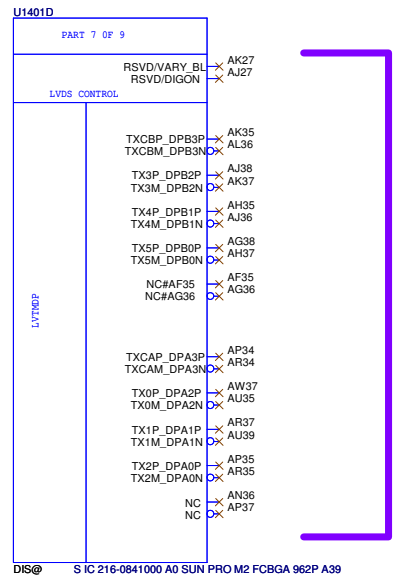
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



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				Date: Tuesday, March 12, 2013 Sheet 16 of 51 <div style="text-align: right; font-size: 1.5em; font-weight: bold;">LA-8126P</div>		



LVDS Interface



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				Date	Tuesday, March 12, 2013
				Sheet	17 of 51

SDV/FVT, NO.11

SDV/FVT, NO.6

+1.8VGS

GPIO 28 FDO	MLPS
H	Disable
L	Enable

+1.8VGS

TSVDD

MarsCRB

Design

120ohm

0.1u

1u

10u

U1401B

PART 2 OF 9

DPA

DPB

DFC

DFD

DAC1

MLPS

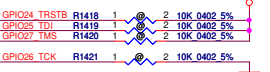
DOCAUX

THERMAL

DIS@

SIC 216-0641000 A0 SUN PRO M2 FCBG4 962P A39

STRAPS



Resistor Divider Lookup Table		
R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	NC	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

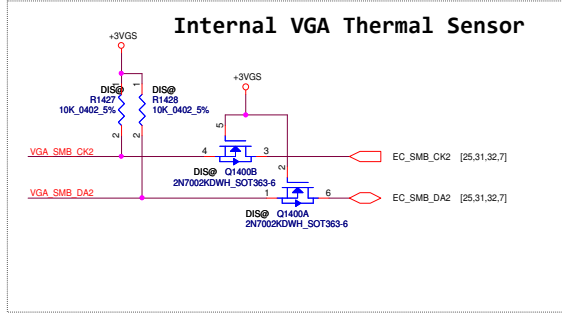
0402 1% resistors are required

Capacitor Divider Lookup Table		
Cap (nF)	Bitd [5:4]	Compal PN
680nF	00	SE00000YJ80
82nF	01	SE076823K80
10nF	10	SE074103KN0
NC	11	

AVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

VDD1DI	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

Internal VGA Thermal Sensor



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

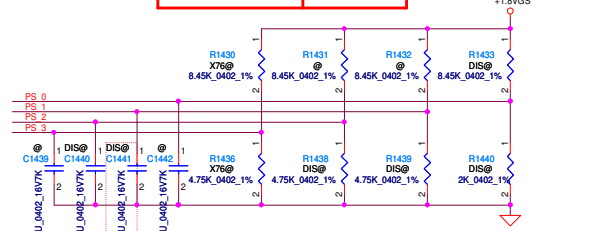
RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1= INSTALL 10K RESISTOR
X= DESIGN DEPENDANT
NA= NOT APPLICABLE

STRAPS	MLPS	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRNS_ENB	PS_1[4]	Transmitter Power Savings Enable 0:50% Tx output swing 1:Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	PCIe Transmitter De-emphasis Enable 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[11]	PCIe Gen3 Enable (NOTE:RESERVED for Thames/Seymour and should be strapped to 0) 0:GEN3 not support at power-on 1:GEN3 supported at power-on	1
BIF_VGA_DIS	PS_2[4]	VGA control 0:VGA controller capacity enabled 1:VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFQ[2:0]	PS_0[3..1]	Serial ROM type or Memory Aperture Size Select If PS_2[3]=0, defines memory aperture size If PS_2[3]=1, defines ROM type 100-512Kbit M2SP05A (ST) 101-1Mbit M2SP10A (ST) 101-2Mbit M2SP20 (ST) 101-4Mbit M2SP40 (ST) 101-8Mbit M2SP80 (ST) 100-512Kbit Pm2SLV010 (Chinghs) 101-1Mbit Pm2SLV010 (Chinghs)	XXX
BIOS_ROM_EN	PS_2[3]	Enable external BIOS ROM device 0:Disabled 1:Enabled	X
AUD[1]	NA	00- No audio function 01- Audio for DP only 10- Audio for DP and HDMI if dongle is detected 11- Audio for both DP and HDMI	XX
AUD[0]	NA	HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	
CEC_DIS	PS_0[4]	Reserved for future ASIC	0
RESERVED	PS_1[3]	Reserved	0
RESERVED	PS_1[2]	Reserved	0
RESERVED	NA	Reserved	0
RESERVED	NA	Reserved (for Thames/Whistler/Seymour only)	0
AUD_PORT_CONN_PINSTRAP[2]	PS_3[5]	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111= 0 usable endpoints 110= 1 usable endpoints 101= 2 usable endpoints 100= 3 usable endpoints 011= 4 usable endpoints 010= 5 usable endpoints 000= 6 usable endpoints 000= all endpoints are usable	XXX
AUD_PORT_CONN_PINSTRAP[1]	PS_3[4]		
AUD_PORT_CONN_PINSTRAP[0]	PS_3[5]		

MLPS Strap

	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[5:1]	1 1	0 0 1	NC	8.45K	2K
PS_1[5:1]	1 1	0 0 0	NC	NC	4.75K
PS_2[5:1]	0 0	0 0 0	680 nF	NC	4.75K
PS_3[5:1]	1 1	X X X	NC	X	X

Mapping to VRAM type please refer to page 04

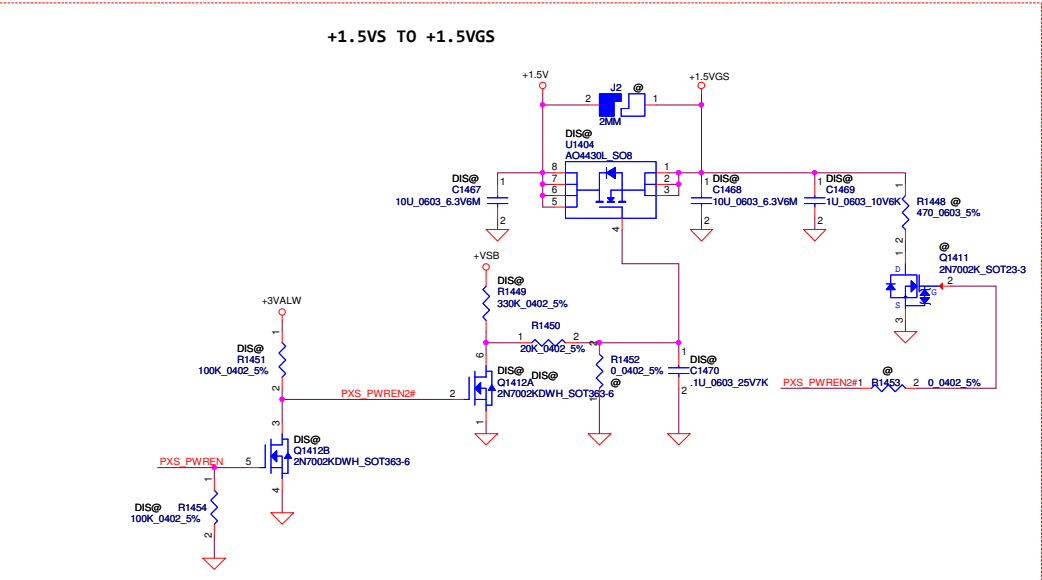
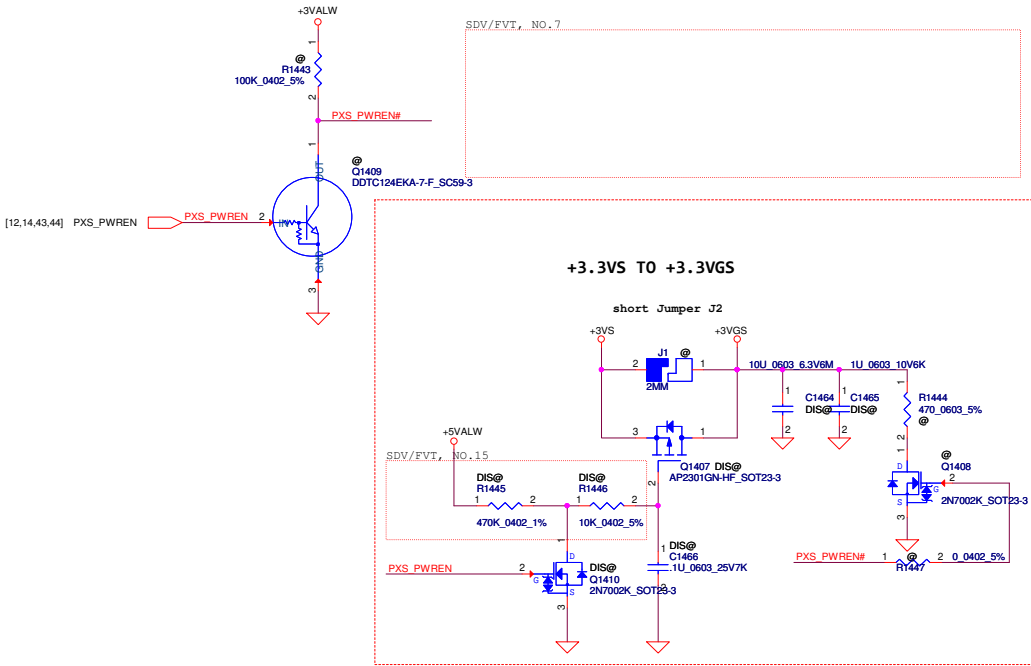
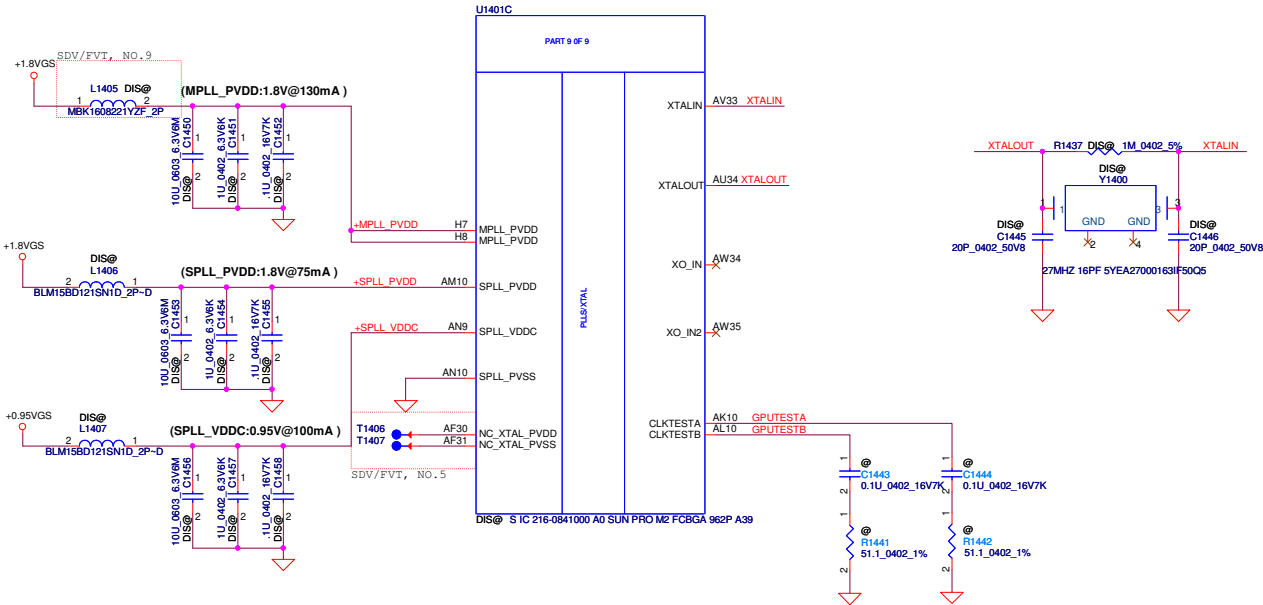


Place CLOSE VGA CHIP

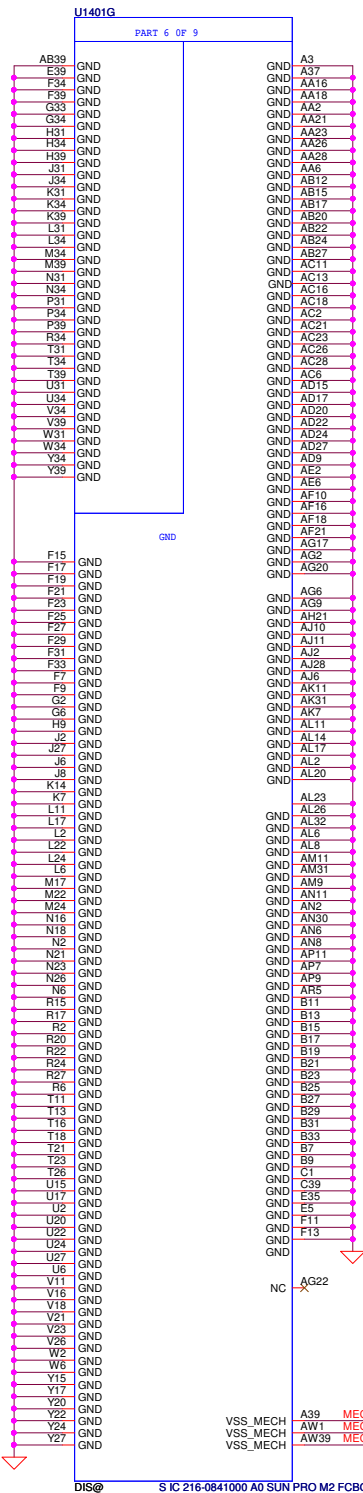
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1



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				LA-8126P
				Date: Tuesday, March 12, 2013
				Sheet 19 of 51

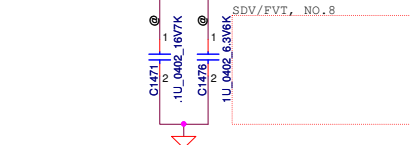


DP_VDDR	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1

AMD:
no display from GPU,
can uninstall the capacitors

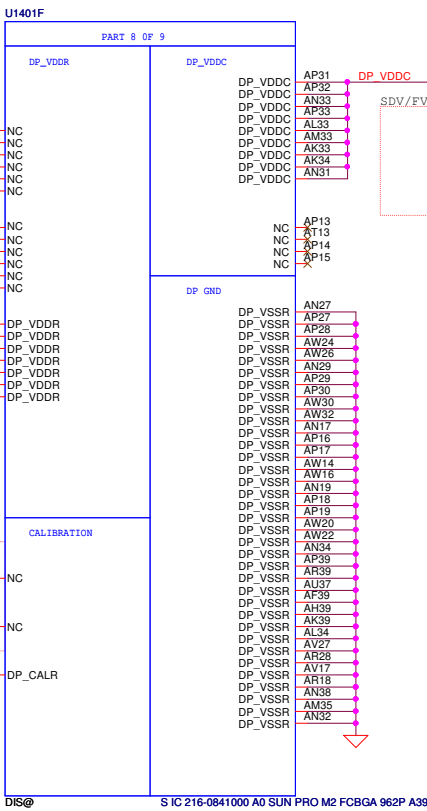
+1.8VGS

(DP_VDDR:1.8V@237mA/link)



SDV/EVT, NO.10

R1459.2 DIS@ 1 150 0402 1% AM39



(DP_VDDC:0.95V@280mA/link)



DP_VDDC	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1

DIS@ S IC 216-0841000 A0 SUN PRO M2 FCBGA 962P A39

VSS_MECH A39 MECH#1 T1403 PAD
VSS_MECH AW39 MECH#3 T1404 PAD
VSS_MECH T1405 PAD

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								AT1 Sun Pro M2 PWR GND					
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Page													
Document Number													
				Custom		LA-8126P		Rev 1.0					
						Date: Tuesday, March 12, 2013		Sheet 20 of 51					

For GDDR5, MVDDQ = 1.5V

(VDDR1:1.5V@3A,GDDR5:1125MHz)

VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	5
1u	0	5
2.2u	5	0
10u	3	5
220u	0	1

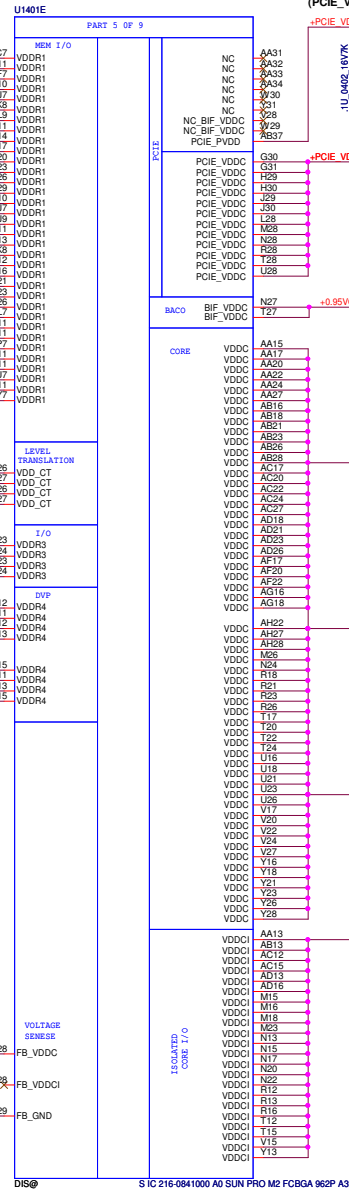
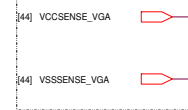
VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	3
10u	1	1

VDDR3	MarsCRB	Design
120ohm	1	0
0.1u	1	0
1u	2	3
10u	0	1

VDDR4	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	0

for Sun Pro Ball name AD12,AF11,AF12,AF13,AF15,AG11,AG13,AG15 is NC

Route as differential pair



(PCIE_VDDR:1.8V@100mA)

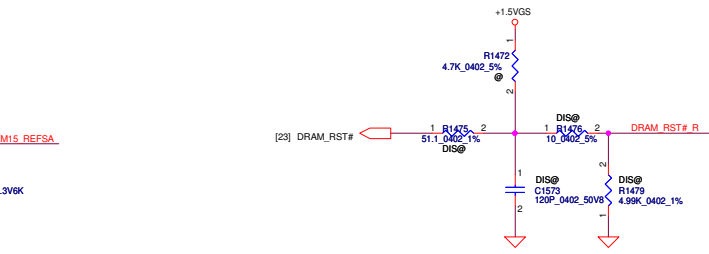
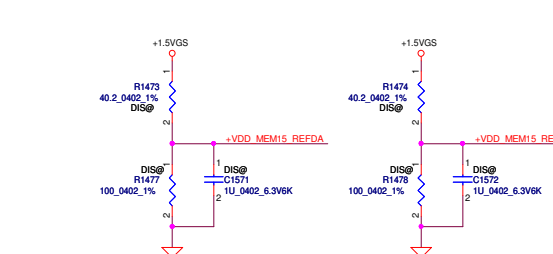
(PCIE_VDDC:0.95V@2.5A_GEN3.0)

(BIF_VDDC:0.95V@1.4A)

(VDDCI:0.9-1.15V@8.8A)

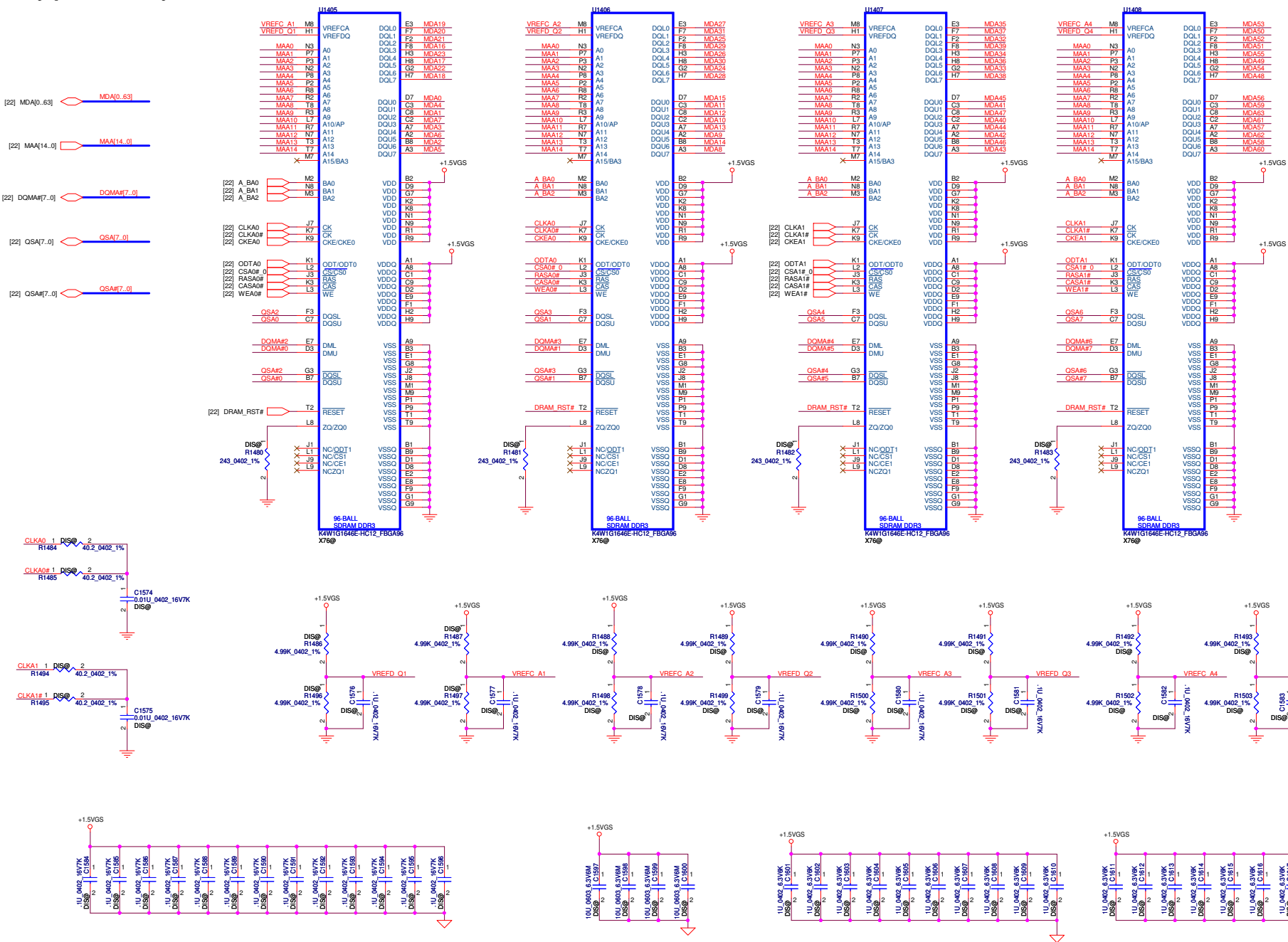
PCIE_VDDR	MarsCRB	Design
0.1u	0	2
1u	2	3
10u	1	1

PCIE_VDDC	MarsCRB	Design
1u	7	5
10u	2	1



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				Size	Document Number	Rev
					LA-8126P	1.0
Date:				Tuesday, March 12, 2013	Sheet	22 of 51

The Seymour M2 only support channel B (64 bit),
this page unmount all parts



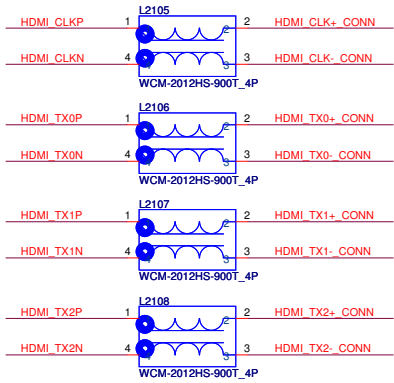
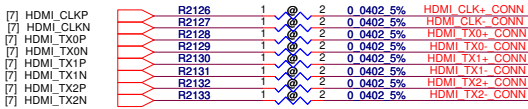
Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i>	
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				Date: Tuesday, March 12, 2013	Sheet 23 of 51

The Mars Pro M2 only support channel B (64 bit)

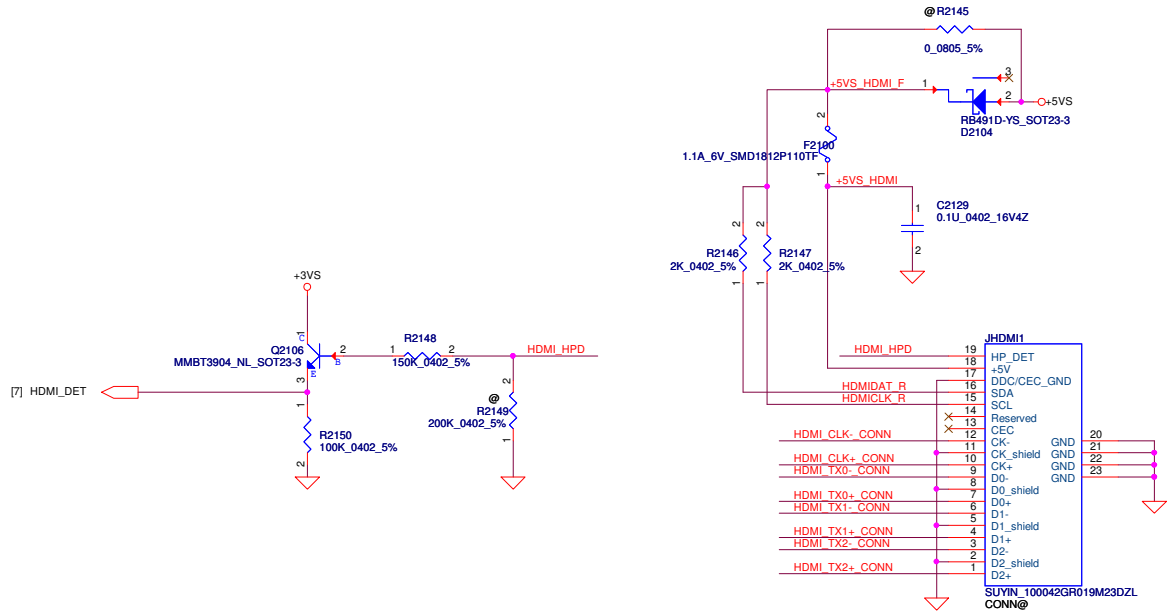
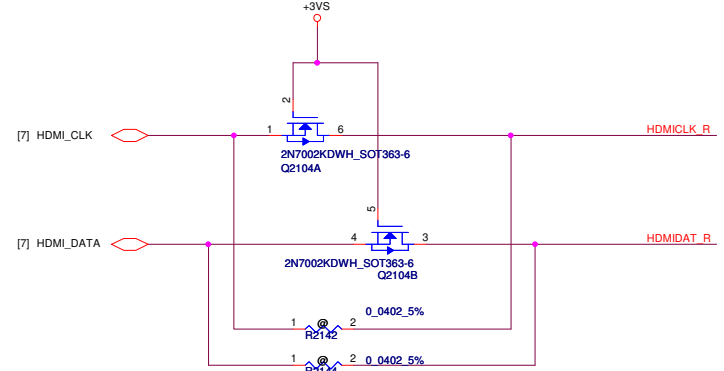
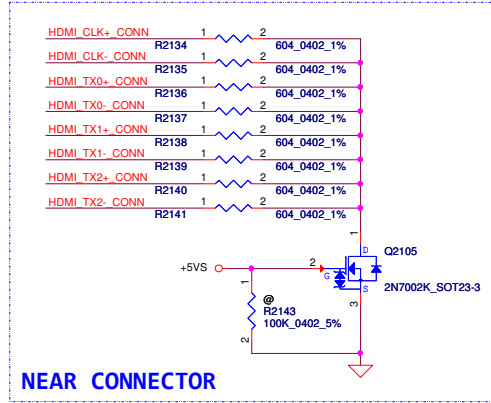
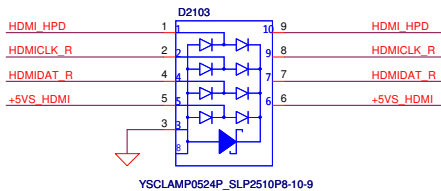
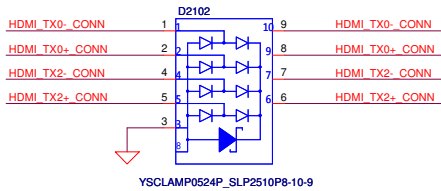
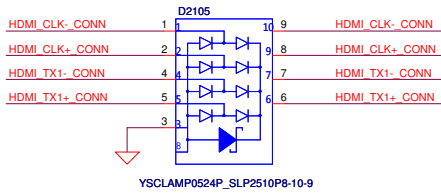
SDV/EVT, No.4

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				C	LA-8126P
Date: Tuesday, March 12, 2013				Sheet	24 of 51
				Rev	1.0

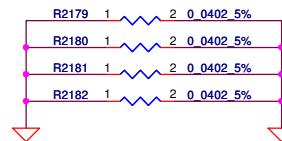
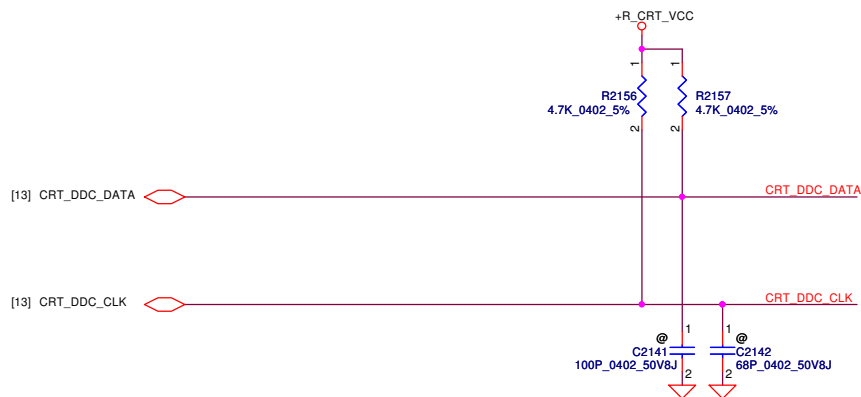
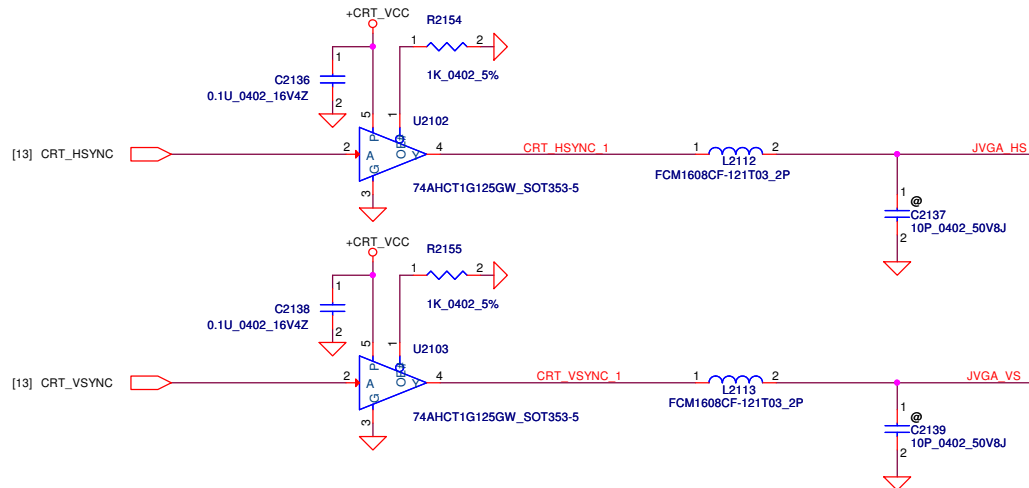
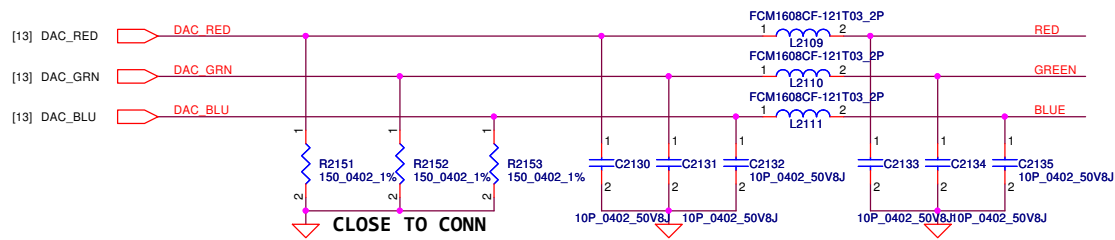
EEROM



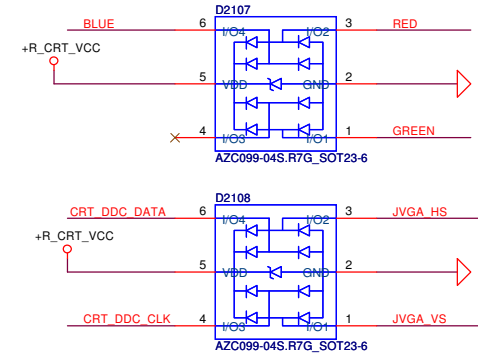
ESD Request



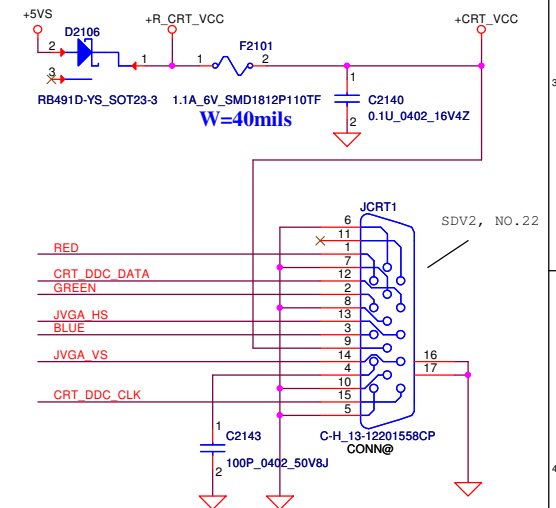
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Date: Tuesday, March 12, 2013		Sheet 27 of 51			



ESD Request



CRT Connector



AMD check list update
20101110

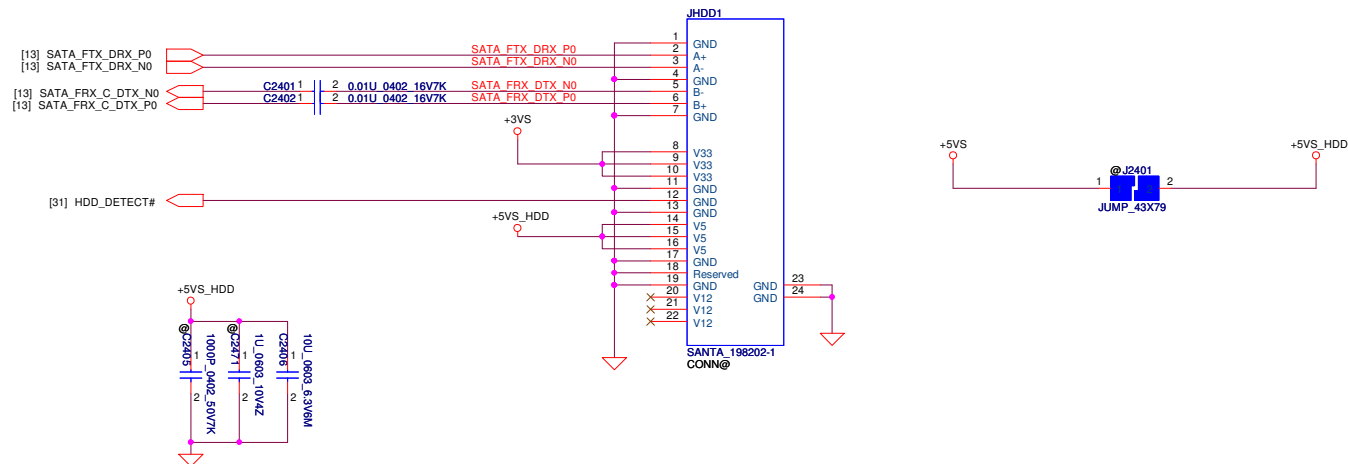
Security Classification		Compal Secret Data				Compal Electronics, Inc.					
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						Size		Document Number		Rev	
						Custom		LA-8126P		1.0	
						Date:		Tuesday, March 12, 2013		Sheet 28 of 51	

CRT Connector

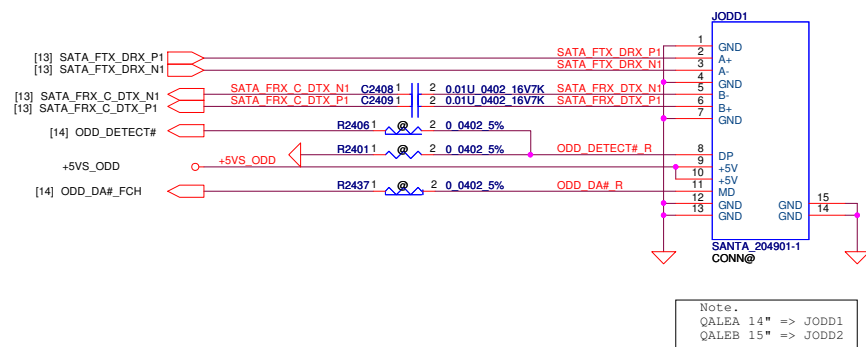
LA-8126P

Rev 1.0

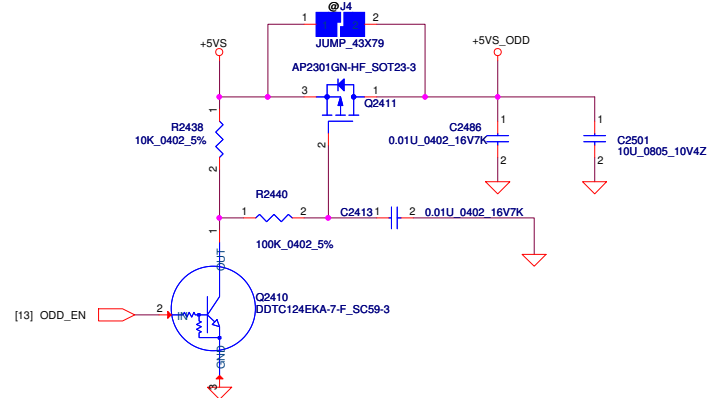
SATA HDD Conn.



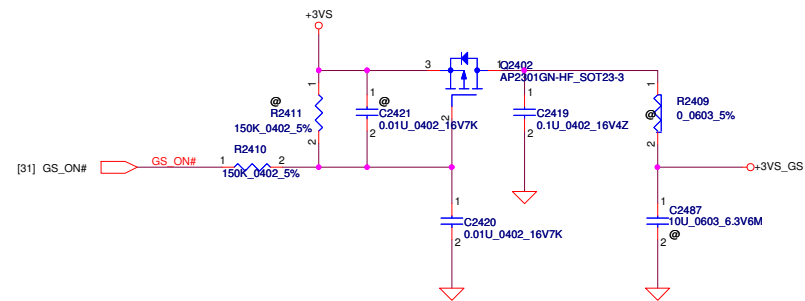
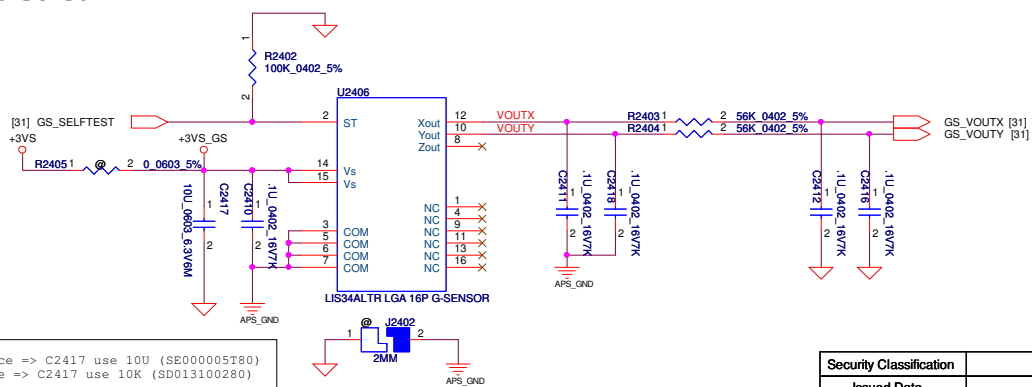
SATA ODD Conn.



ODD Power Control

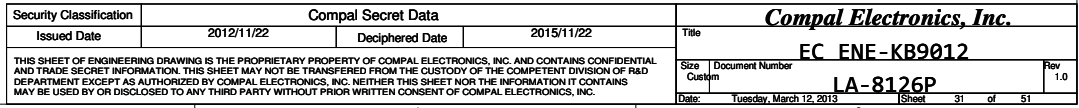


APS G-Sensor

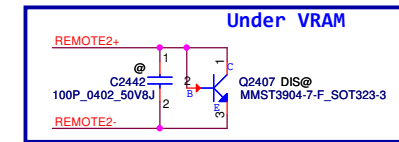
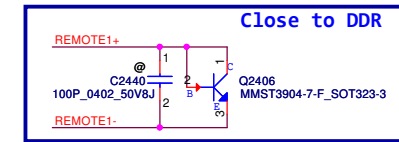
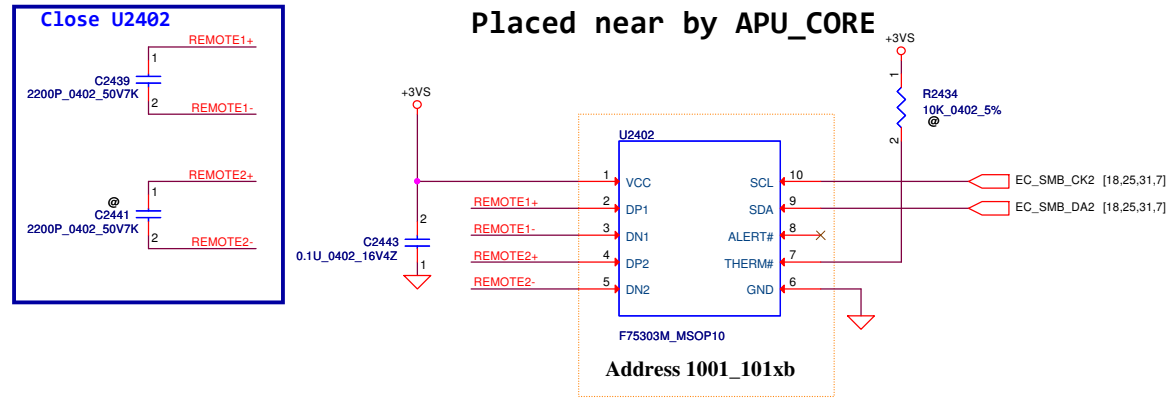


Note.
Main Source => C2417 use 10U (SE000005T80)
2nd Source => C2417 use 10K (SD013100280)

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						Document Number	LA-8126P	Rev	1.0
						Date	Tuesday, March 12, 2013	Sheet	30 of 51

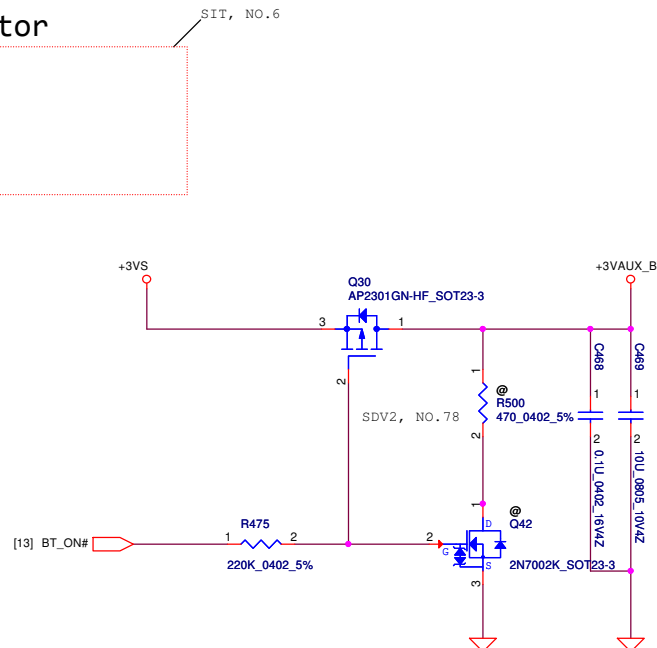


Fintek Thermal sensor Placed near by APU_CORE

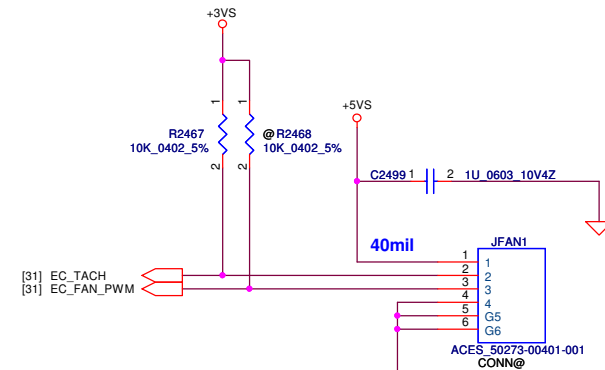


REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

BT Connector

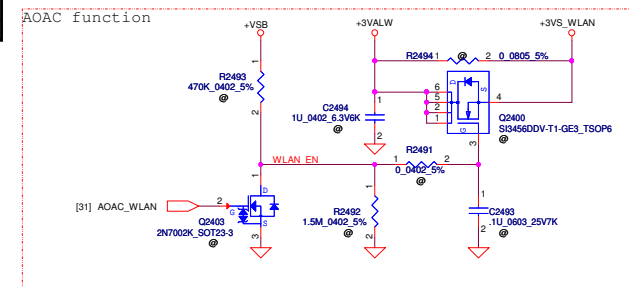
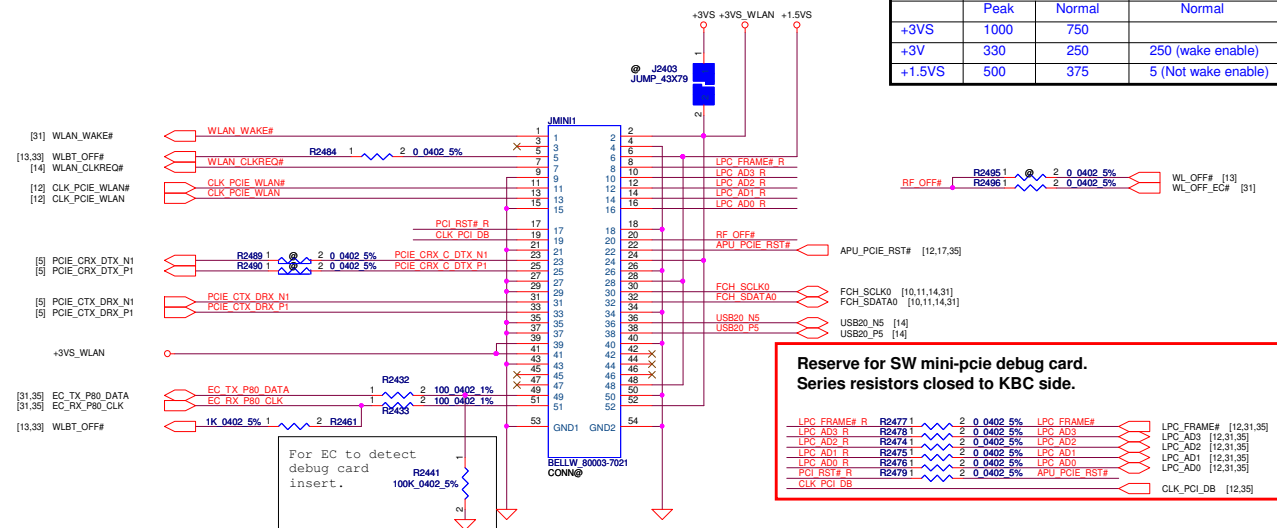


FAN1 Conn



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				LA-8126P	
				Date:	Rev 1.0
				Tuesday, March 12, 2013	Sheet 32 of 51

WLAN Conn



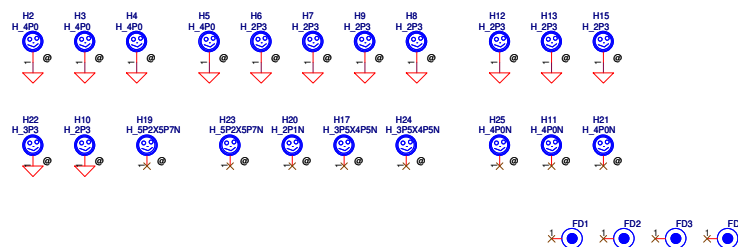
For AOAC assessment

- +3VS_WLAN path:
- 1. +3VS (default)
- 2. +3VALW
- 3. +3VALW + Switch

INT_KBD Conn.



Screw Holes



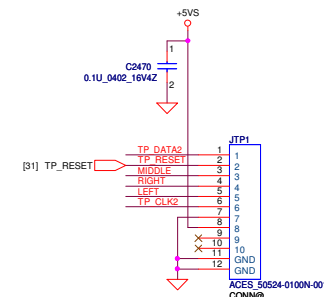
ZZZ3



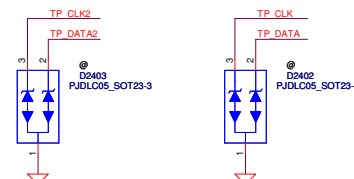
LA-8126_PCB

DA8000XQ010

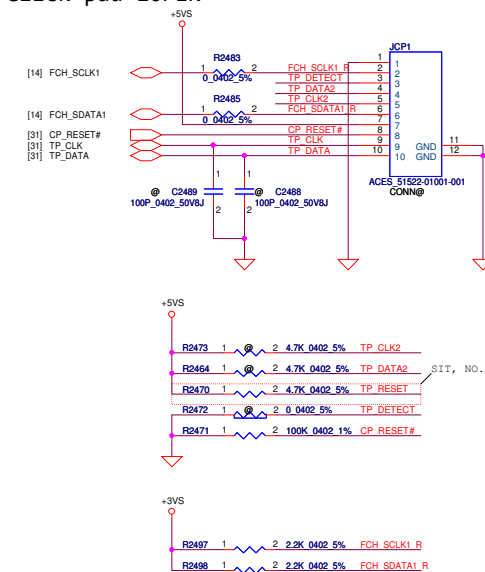
Track Point Conn



ESD Request

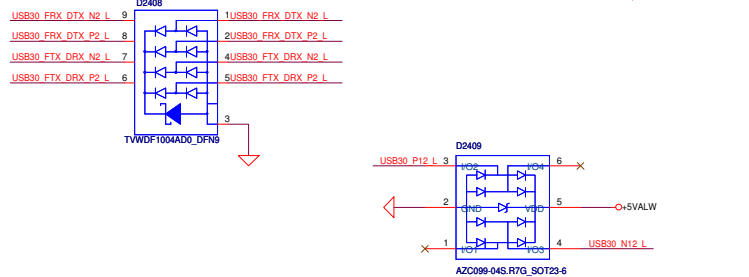
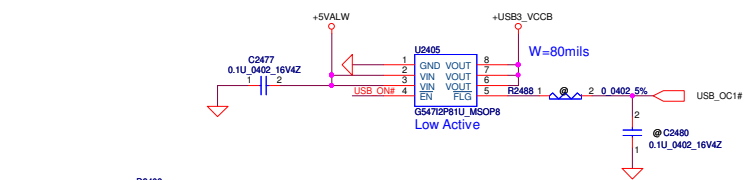
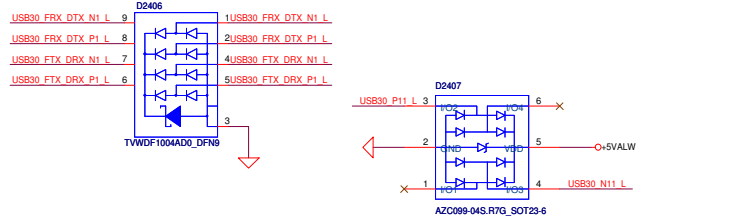
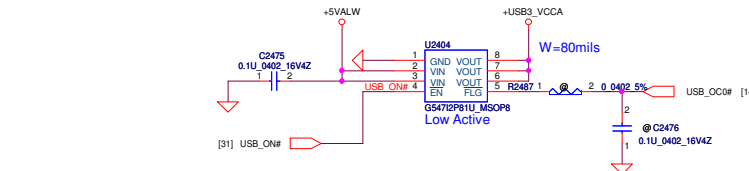
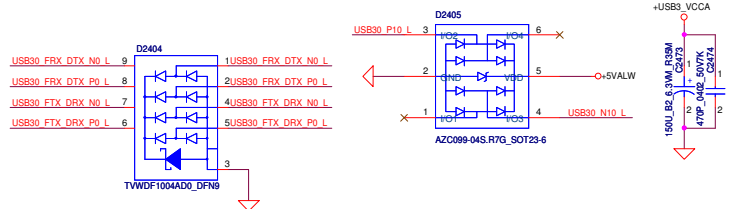
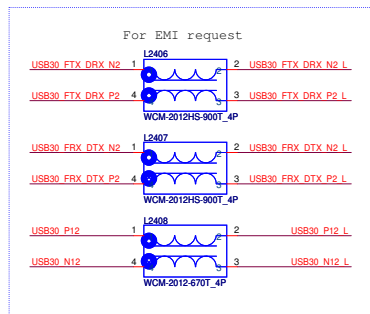
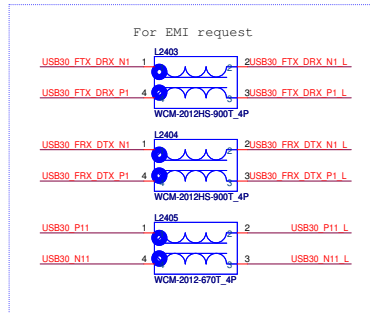
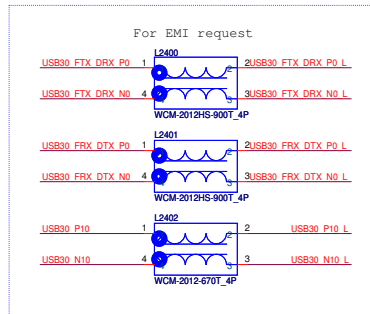
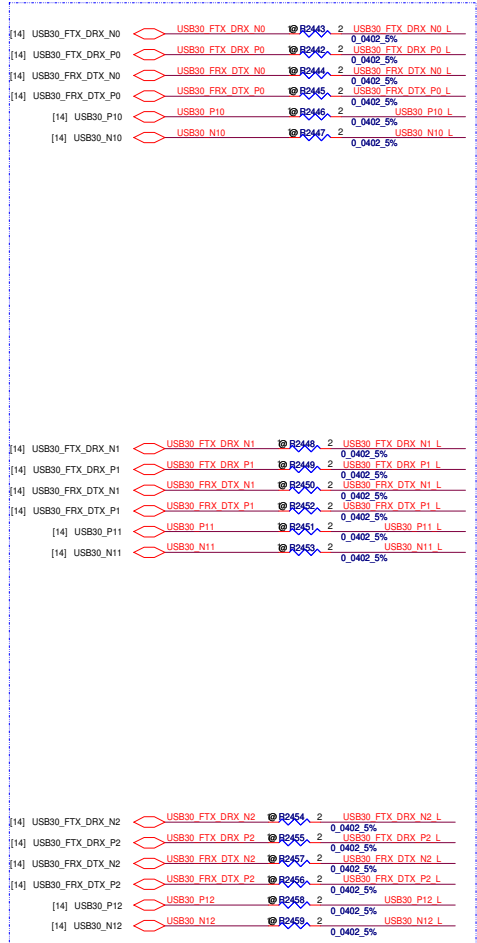


Click pad 10PIN

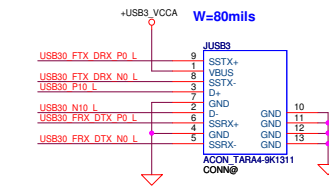


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				LA-8126P	Rev 1.0
				Version	2012.10.10
				Page	95 of 51

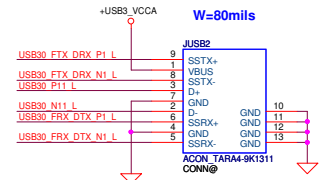
USB3.0 Conn *3



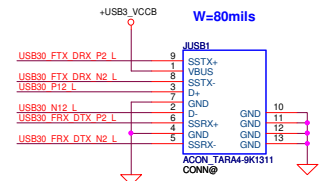
LP1



LP2

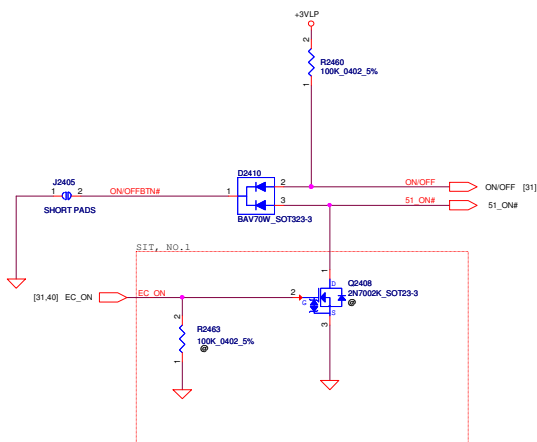


LP3

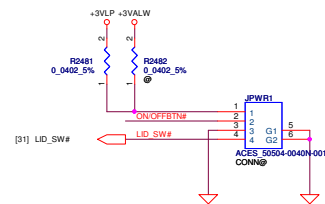


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Size C	Document Number	LA-8126P		Rev 1.0
Date:	Tuesday, March 12, 2013	Sheet	34 of 51	

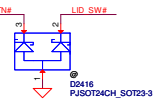
ON/OFF switch



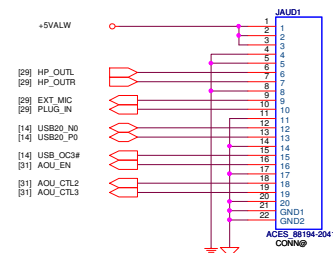
Power Button Board Conn



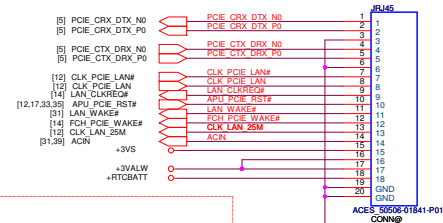
ESD Request



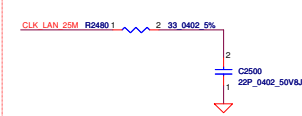
USB2.0/Audio Jack SB CONN



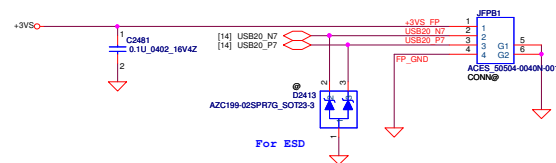
Lan Conn



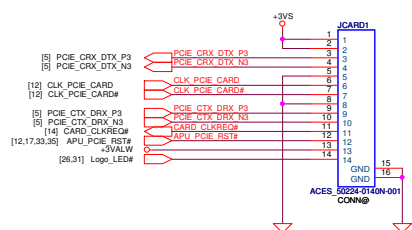
ESD Request



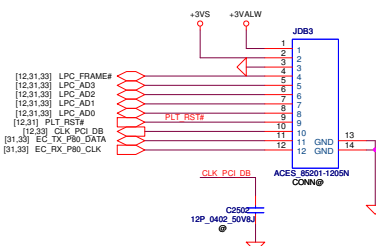
Finger Printer



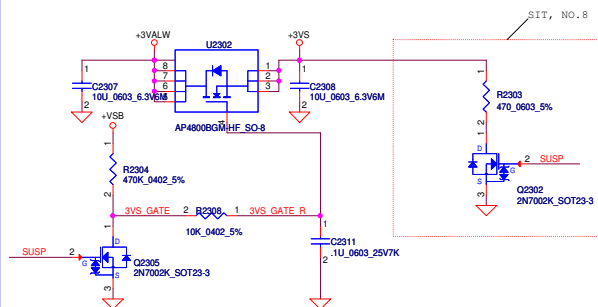
Card Reader



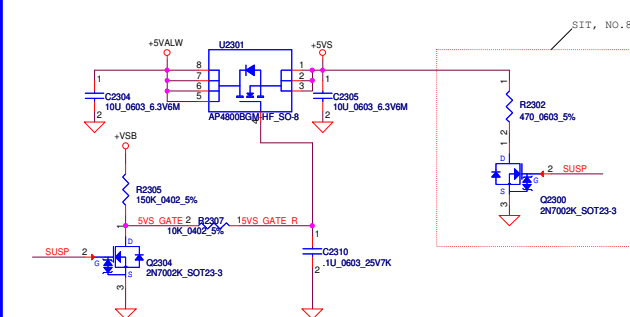
Debug Conn.



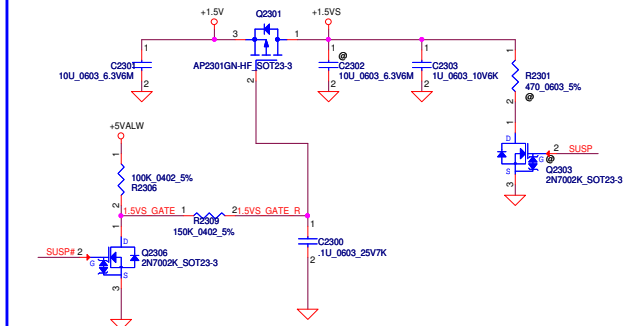
+3VALW TO +3VS



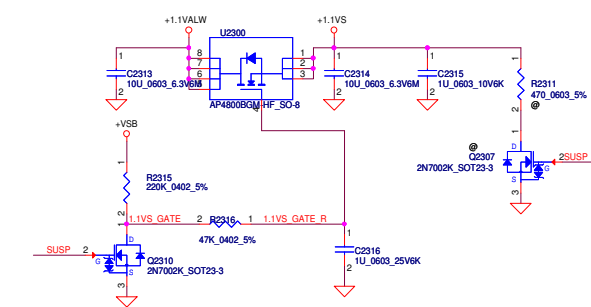
+5VALW TO +5VS



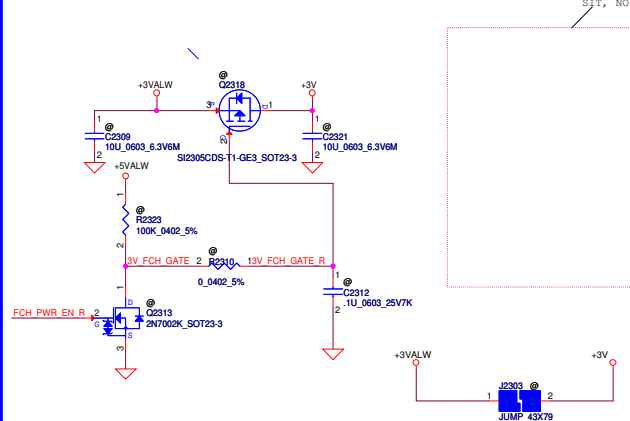
+1.5V to +1.5VS



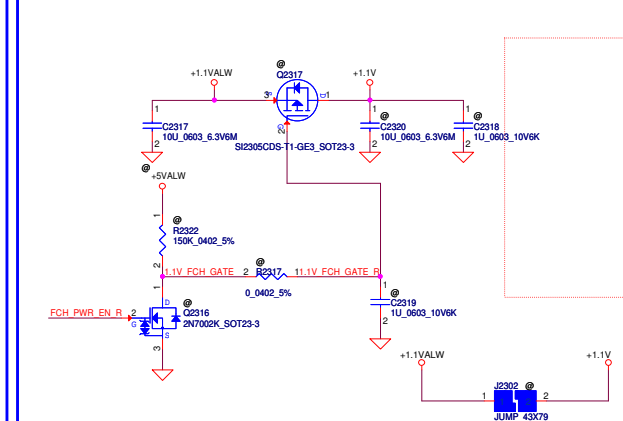
+1.1VALW to +1.1VS



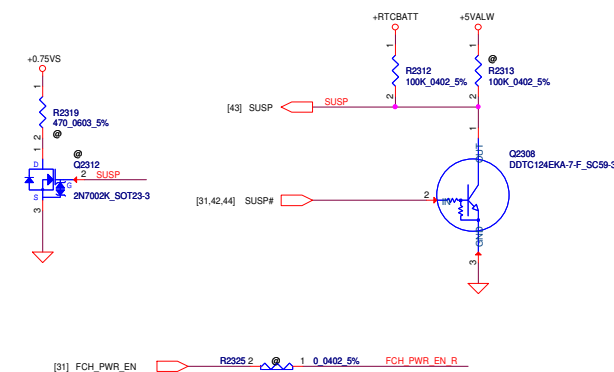
+3VALW TO +3V



+1.1VALW to +1.1V

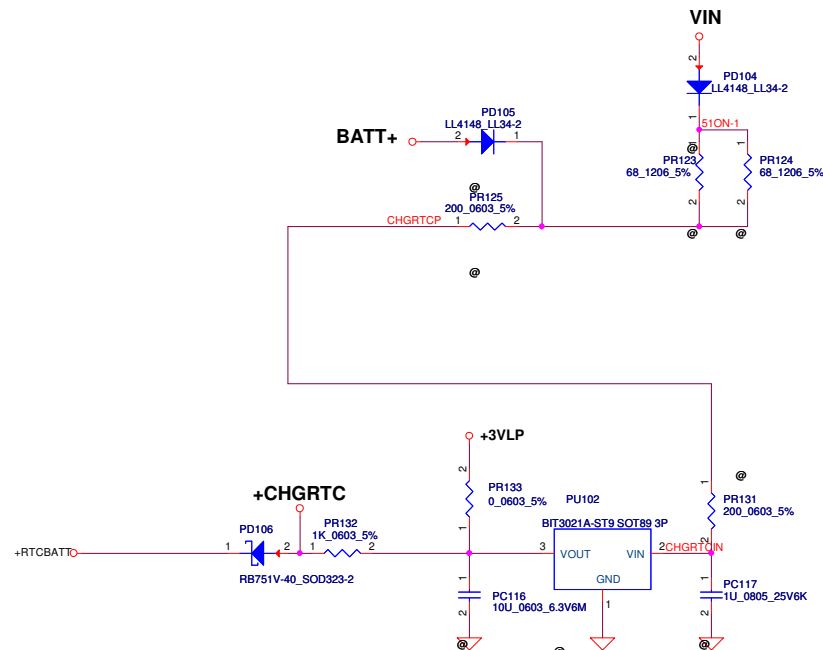
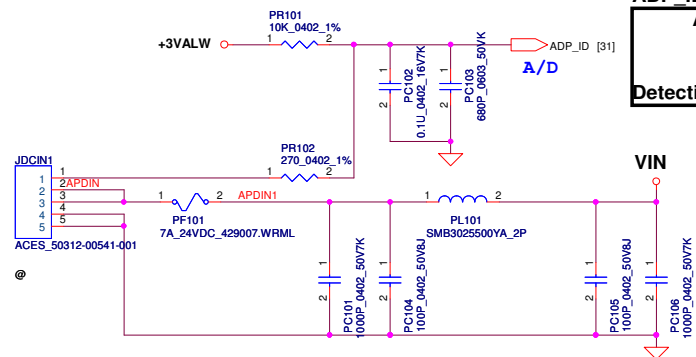


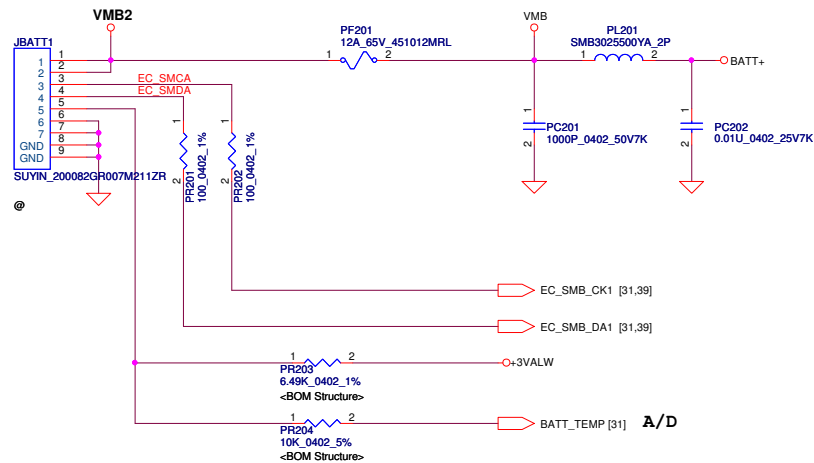
+3VALW TO +3V_FCH



ADP_ID

AC Adapter	135W	90W	65W
R(K ohm)	0	open	10
ADP_ID(V)	0	3.3	1.65
Detection voltage	<0.33	>2.64	1.32~1.98

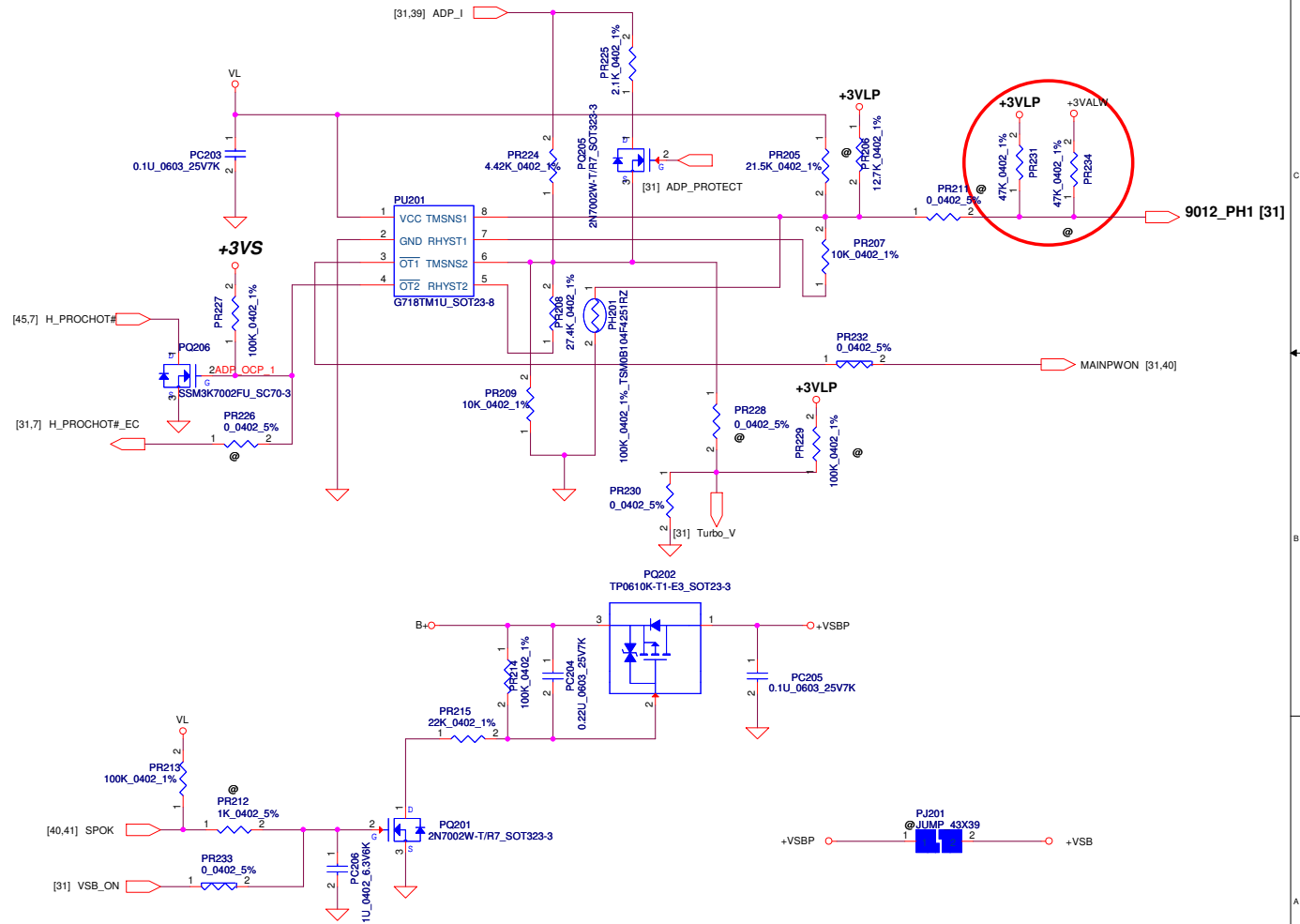




PH1 under CPU bottom side :
CPU thermal protection at 93 \pm 3 degree C
Recovery at 56 \pm 3 degree C

For KB930 --> Keep PU201 circuit
(Vth = 1.25V)

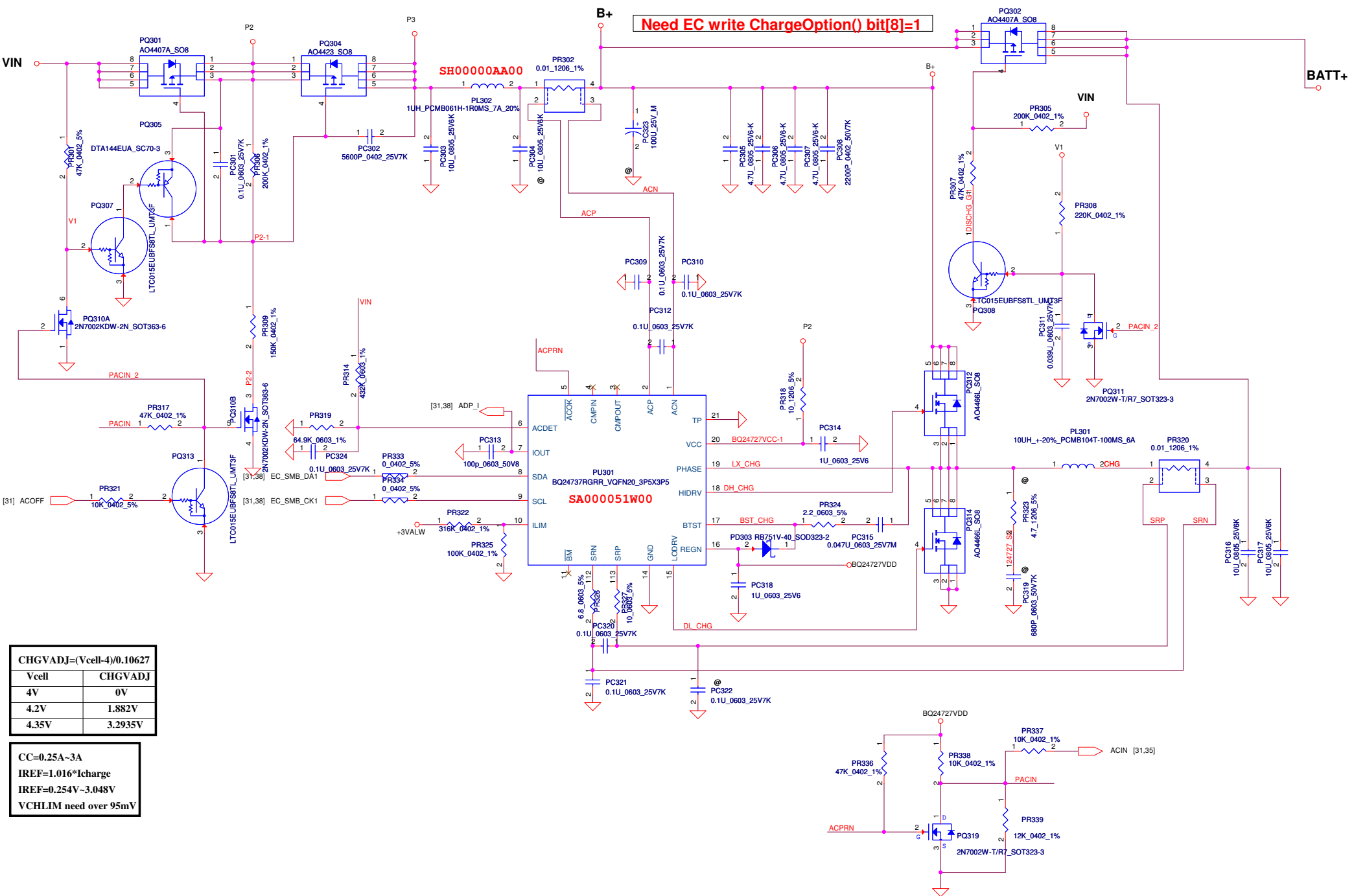
For KB9012 (Red square) --> Remove PU201 circuit, but keep PR206
PH201



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Date: Tuesday, March 12, 2013				Sheet 38 of 51

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PWR-BATTERY CONN/OTP

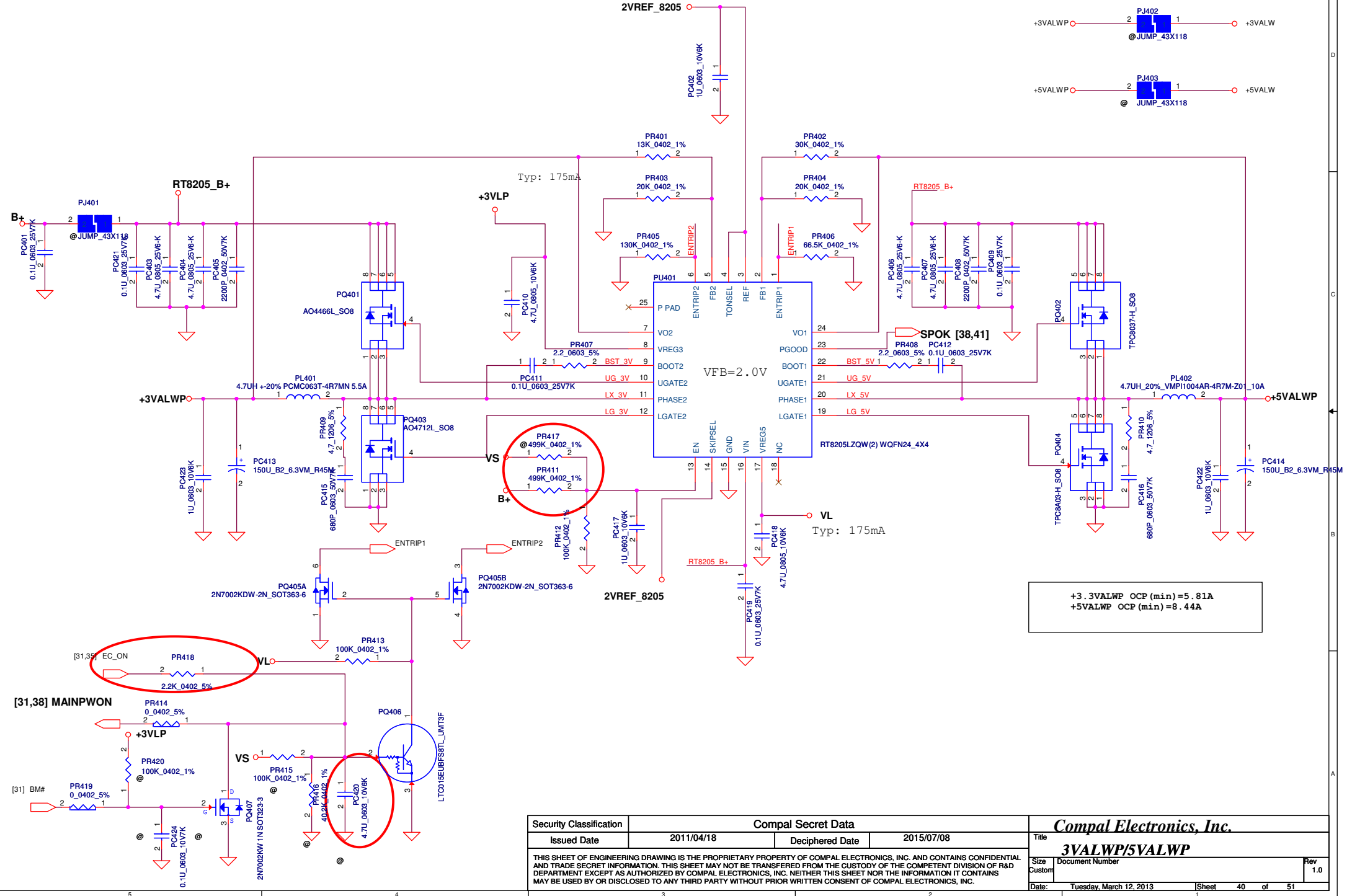


CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

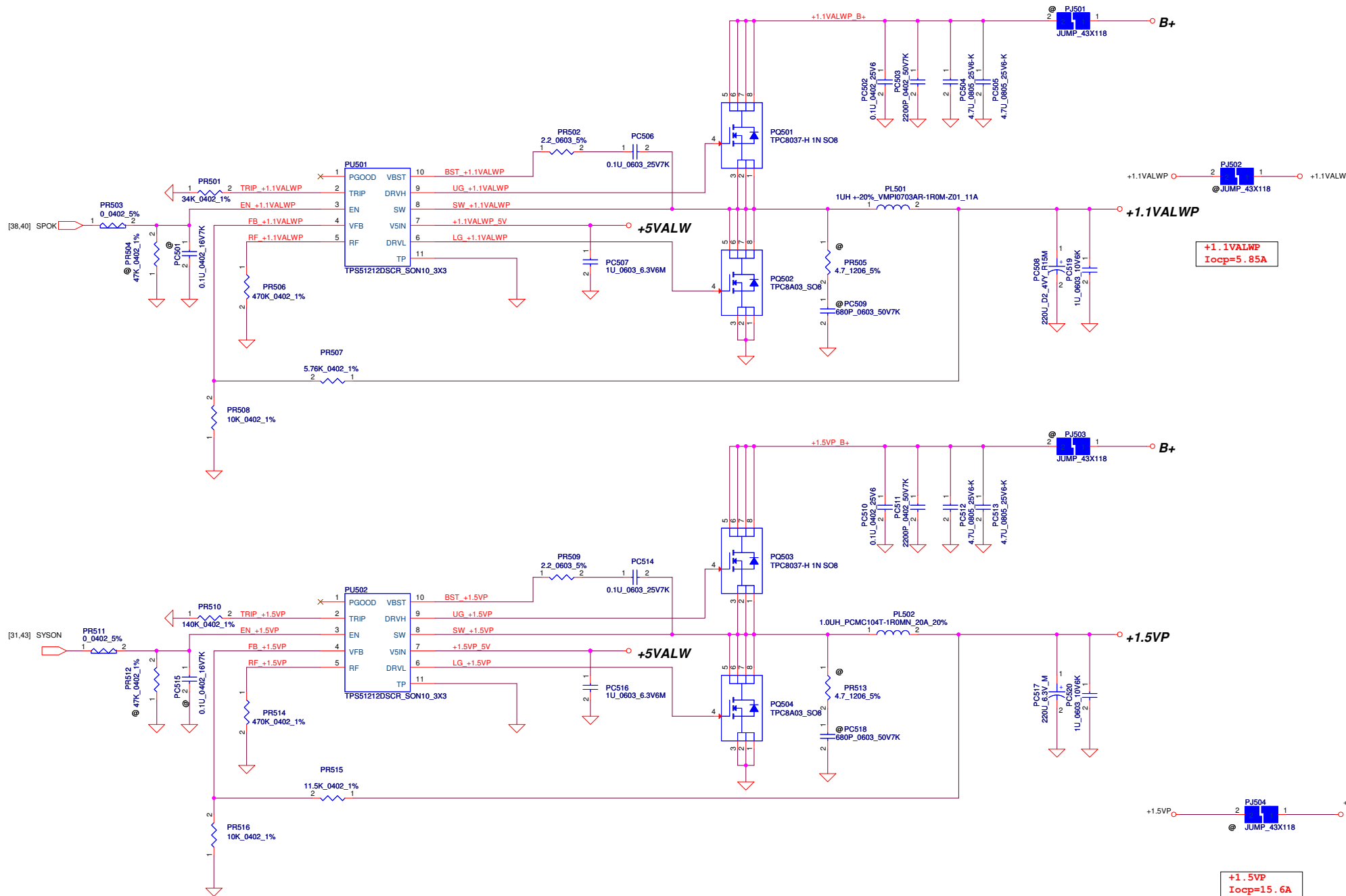
CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

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				Sheet	39 of 51
				Rev	1.0

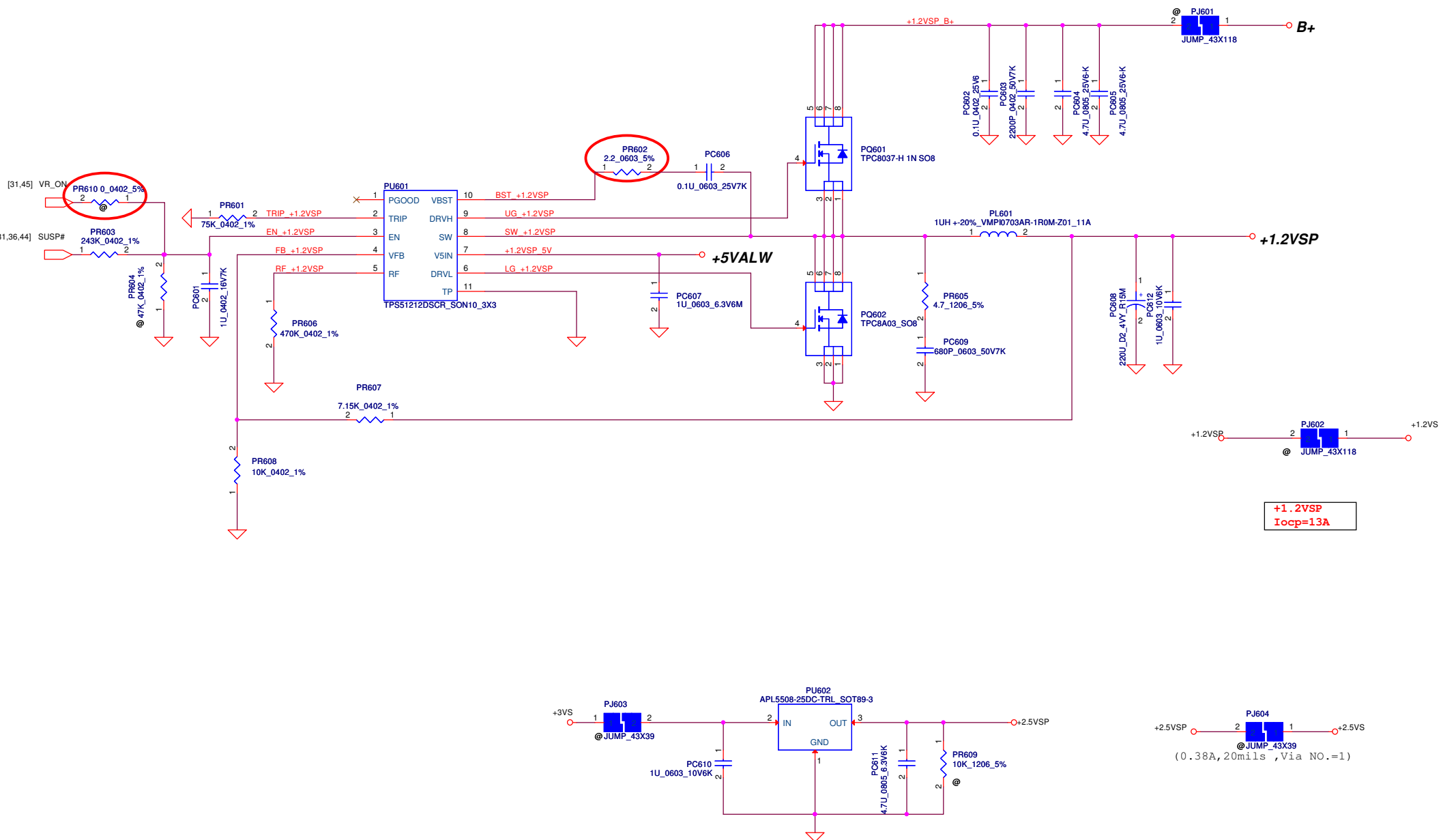
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



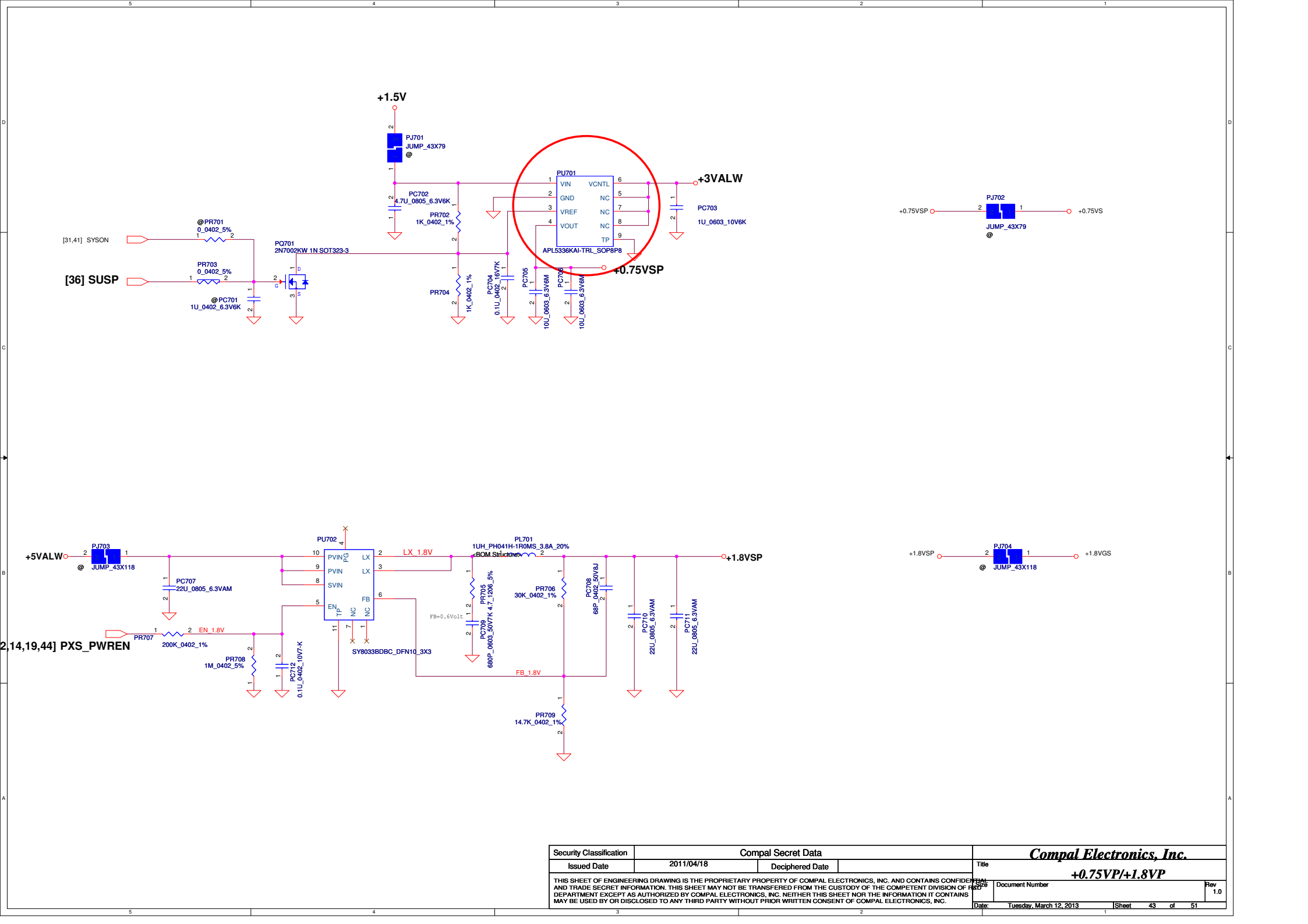
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				Date	Tuesday, March 12, 2013
				Sheet	40 of 51
				Rev	1.0



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Date: Tuesday, March 12, 2013			Sheet 41 of 51	



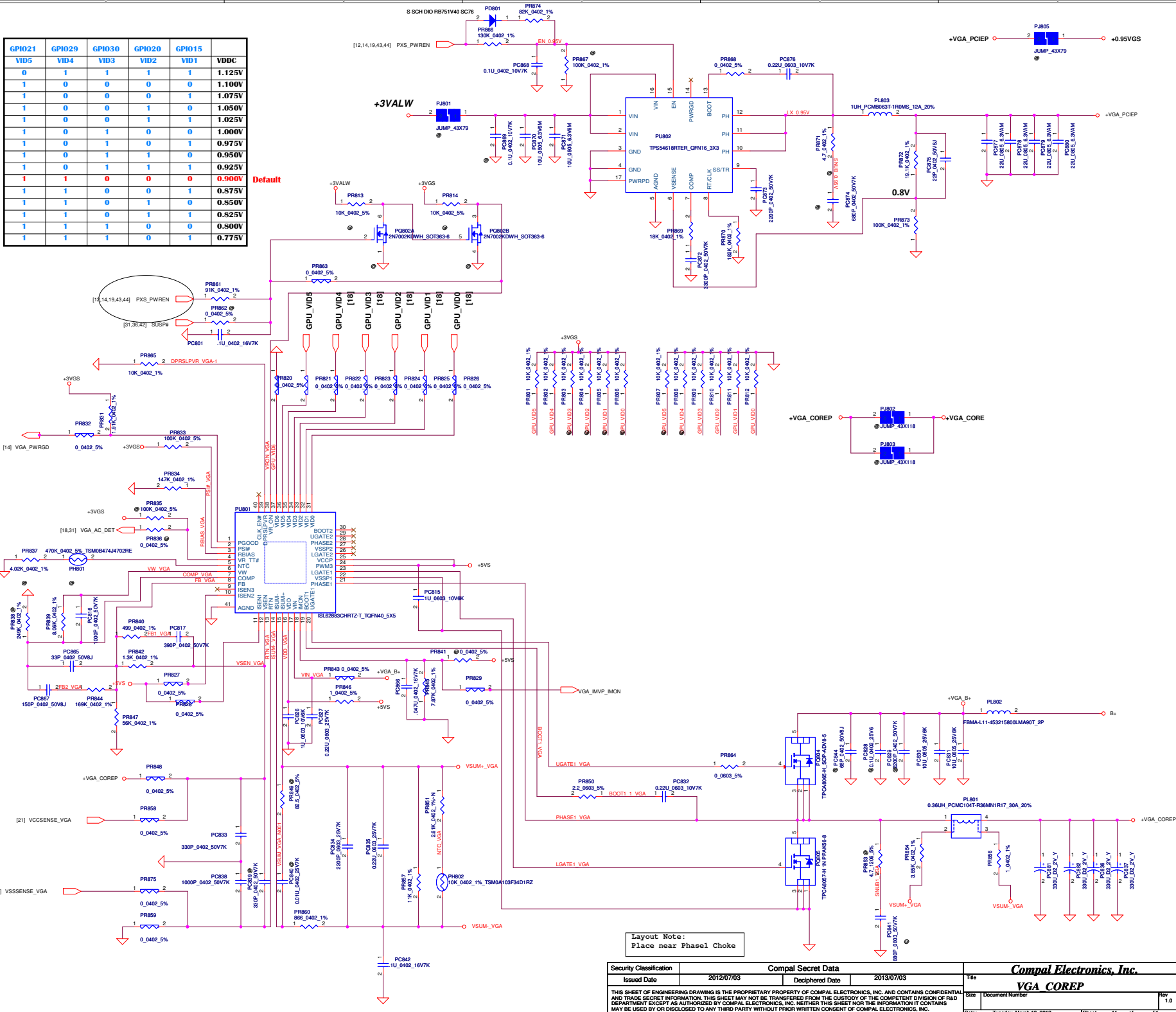
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+1.2VSP/+2.5VSP					
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		Rev		1.0	
Date:		Tuesdav, March 12, 2013		Sheet 42 of 51	



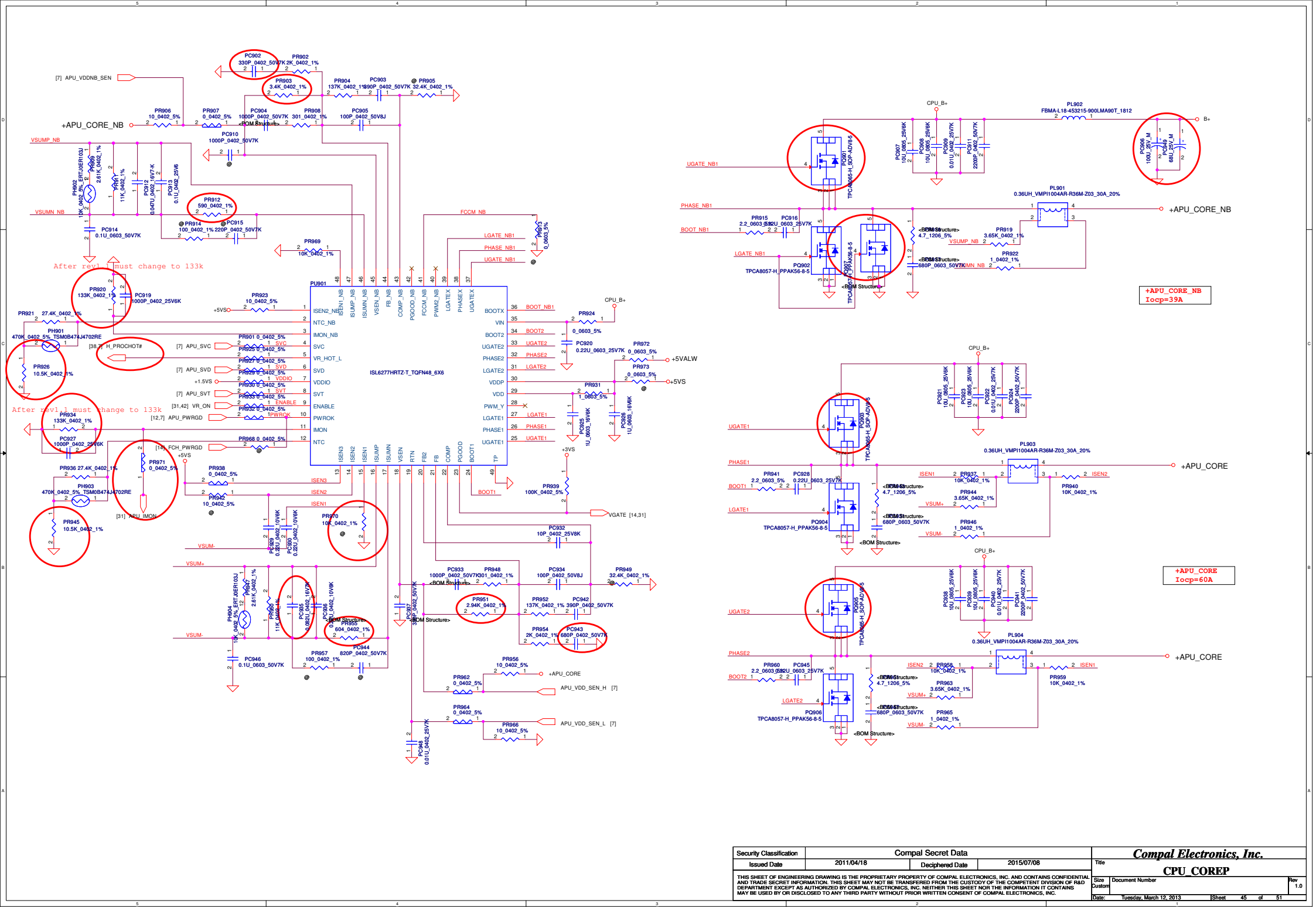
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				Date: Tuesday, March 12, 2013	Sheet 43 of 51

GPIO21	GPIO29	GPIO30	GPIO20	GPIO15	VDDC
VID5	VID4	VID3	VID2	VID1	
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	1	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	1	0.800V
1	1	1	1	1	0.775V

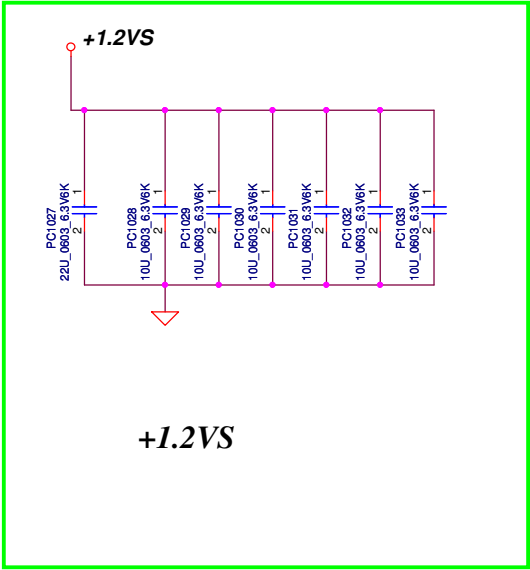
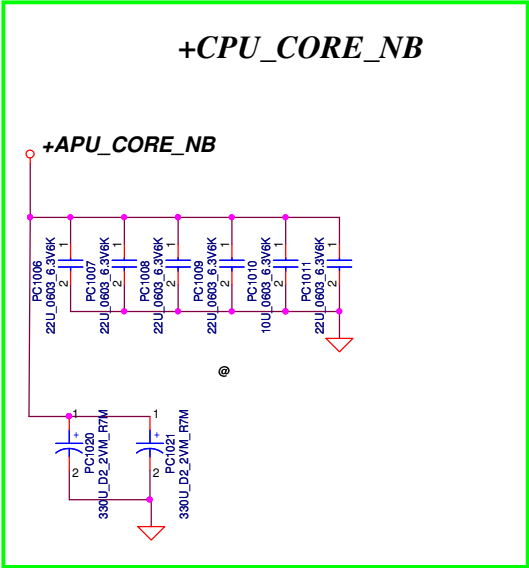
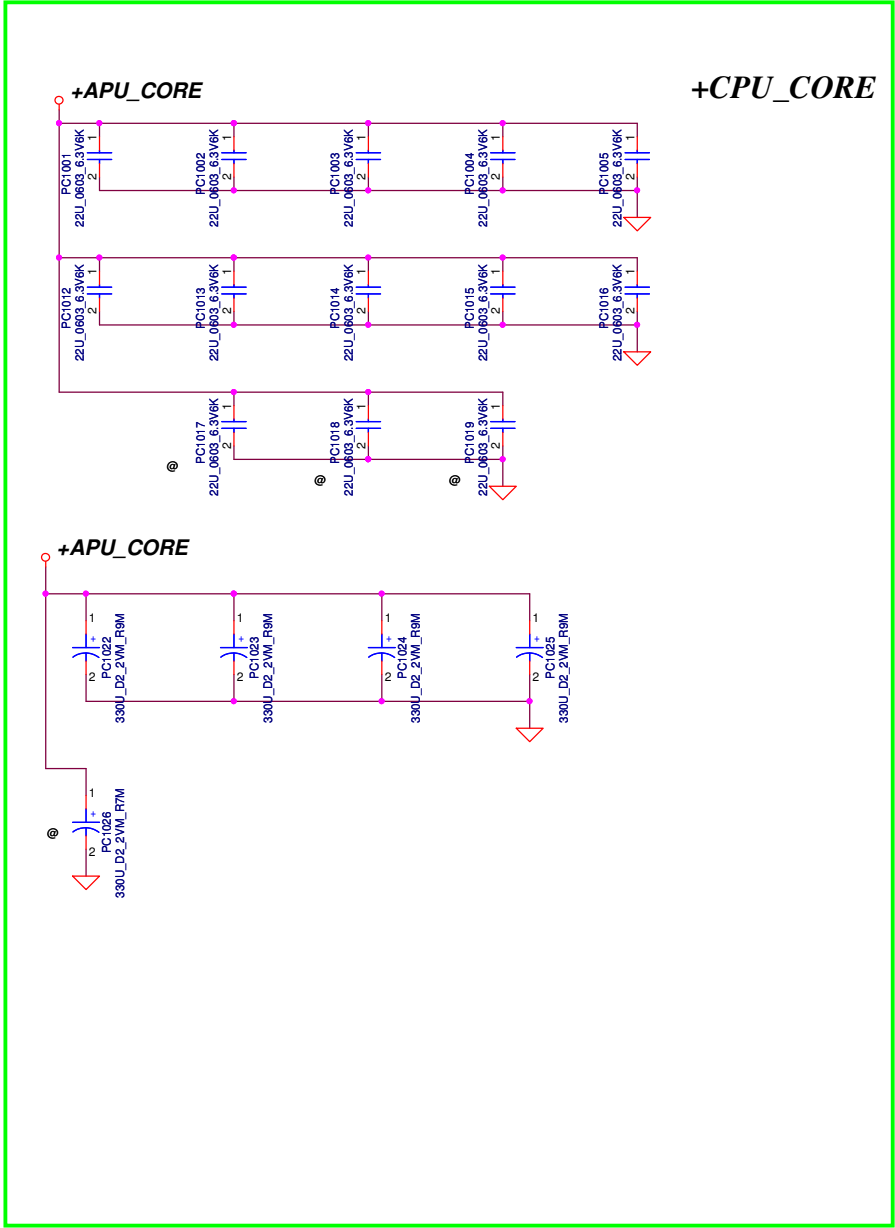
Default



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Date: Tuesday, March 12, 2013				Sheet	44 of 51



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Date		Tuesday, March 12, 2013		Sheet	45 of 51



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Size A3	Document Number				Rev 1.0	
Date:		Tuesday, March 12, 2013		Sheet 46	of 51	

Version change list (P.I.R. List)

Page 1 of 1
for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	Base on EE's request for fine tune power sequence.	P44	Change PR866 from 2.49k to 130k.	2013.1.11	From 0.1 to 0.2
2	For fine tune OCP set up point of VGA core.	P44	Change PR860 from 604ohm to 866ohm.	2013.1.11	From 0.1 to 0.2
3	Base on EE's request for fine tune power sequence.	P44	Change PR861 from 47k to 91k.	2013.1.11	From 0.1 to 0.2
4	Base on must meet EUP spec, change power design.	P37	Remove PR110, PC108, PR114, PC109, PR109, PC107,PU101, PR111, PD101, PR138, PR116, PR112, PD105, PR125, PR128, PC114, PR129, PQ101, PD104, PR123, PR124, PC115, PR131, PC117, PR103, PR104, PR105, PD102, PQ102, PR106, PR107, PQ103, PQ104, PR108, PR118, PR121, PC113, PR127, PQ106, PQ105, PR120, PR115, PC110, PC112, PR126, PR119, PR122, PD103.	2013.1.11	From 0.2 to 0.3
5	Base on must meet EUP spec, change power design.	P39	RemovePQ315, PR328, PR329, PQ316, PD304, PD301, PD302, PQ303, PR303, PR304, PQ306, PQ309.	2013.1.11	From 0.2 to 0.3
6	Base on must meet EUP spec, change power design.	P39	Add PR336, PR338, PR337, PR339, PQ319.	2013.1.11	From 0.2 to 0.3
7	Base on must meet EUP spec, change power design.	P40	Remove PR417, PC420, PQ407, PR420, PC424. Add PR411. Change PR418 from 47K to 2.2K.	2013.1.11	From 0.2 to 0.3
8					
9					
10					
11					
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				Size Custom Document Number C38-G series Chief River Schematic ^{1.0} Rev	
Date: Tuesday, March 12, 2013				Sheet 47 of 51	

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	S		4		3		2		1
	Phase	Date	No.	BOM	Sch	Layout	Description		
D									
C									
B									
A									

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Date:				Tuesday, March 12, 2013	Sheet 50 of 51 Rev 1.0

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